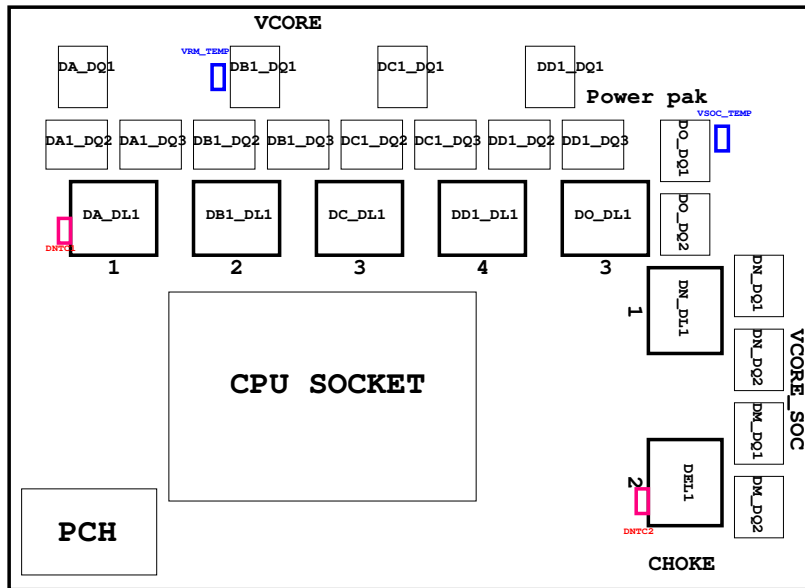



A520M H

PAGE	TITLE	Revision : 1.0
01	COVER SHEET	
02	BOM & PCB MODIFY HISTORY	
03	BLOCK DIAGRAM	
04	CPU DDR4 MEMORY	
05	CPU CONTROL	
06	CPU GFX, GPP, SB, GND	
07	CPU MISC	
08	CPU POWER & GND	
09	CPU CLK/SPI/USB	
10	DDR4 CHANNEL A	(X57_R0.5)
11	DDR4 CHANNEL B	(X57_R0.5)
12	PM CLK/GPIO/FAN	
13	PM USB	
14	PM UMI/GPP/SATA	
15	PM POWER & GND	
16	IT8688	(X57_R1.09)
17	PCI EXPRESS x16	
18	REALTEK ALC887	(REV0.5)
19	REAR AUDIO JACK	(REV0.5)
20	PWM RAA229004	(REV0.13)
21	VCORE MOS1	(REV0.13)
22	VCORE MOS2	(REV0.13)
23	POWER SEQUENCE , A_VDDP	
24	DDR POWER , 5VDUAL	
25	VPPMEM , OC DAC	

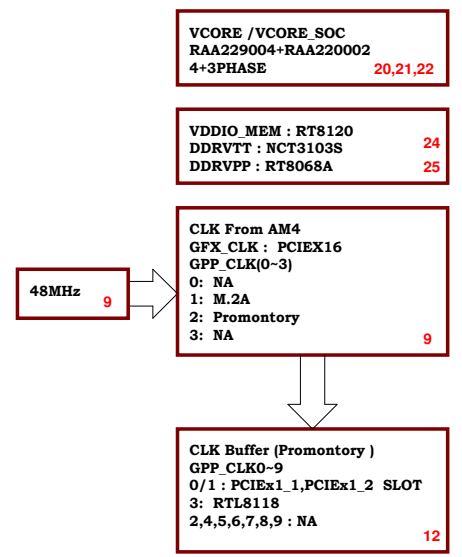
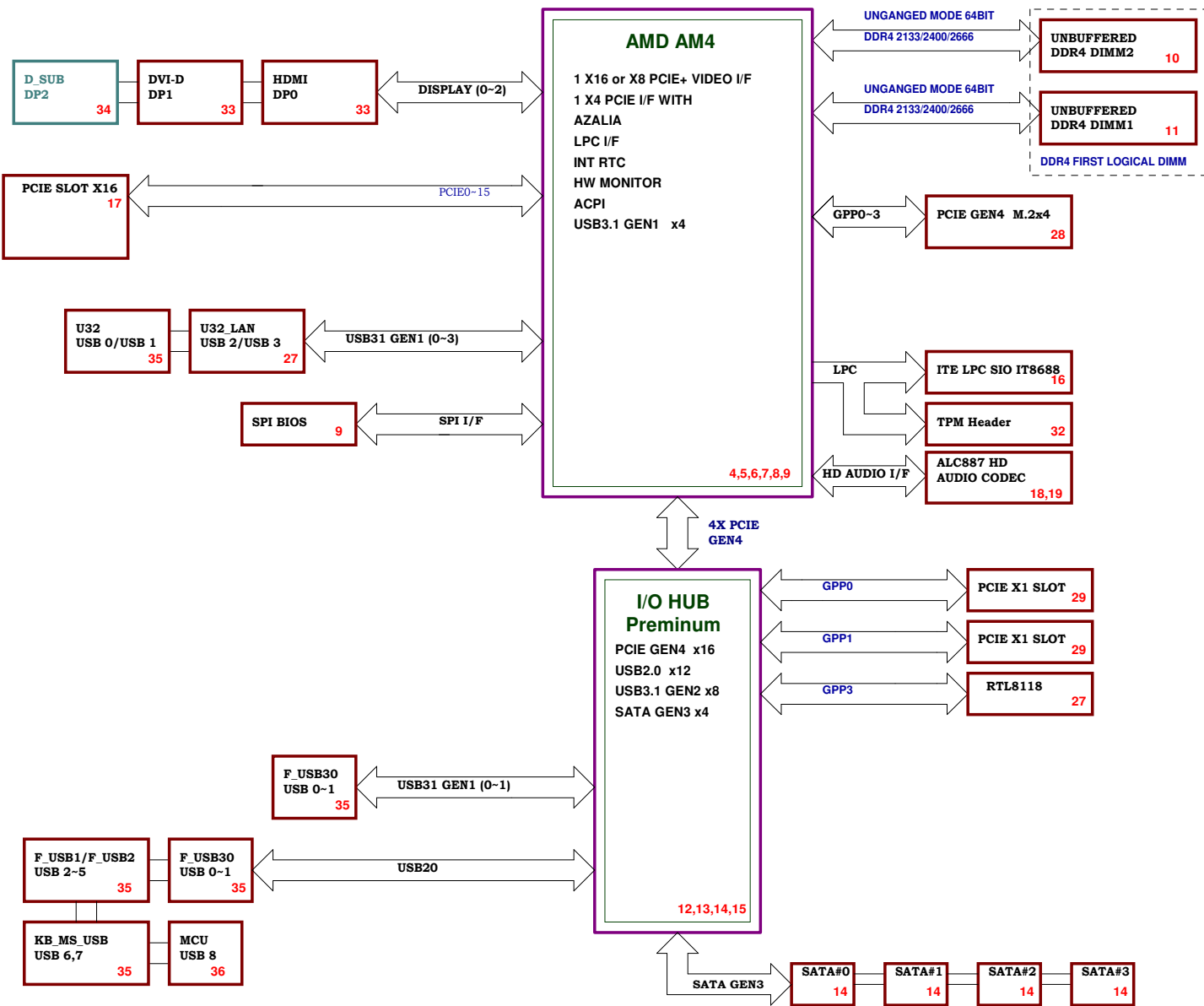
PAGE	TITLE
26	A_VDD1V8
27	REALTK RTL8118 (X57_R2.03)
28	M2A (X57_R0.5)
29	PCI EXPRESS x1
30	TOP , ARMOR , HS
31	CPU SMD CAP BOTTOM
32	FAN , COM , HWM , TPM
33	HDMI,DVI
34	VGA (X57_R1.03)
35	F_USB , F_USB30 , R_USB30 , KB_MS_USB
36	IT5702 (REV1.0)
37	CPU / IO / DDR LED / C_LED (REV1.0)
38	D_LED (REV1.0)
39	ATX , F_PANEL (REV1.0)

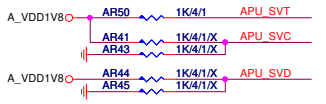
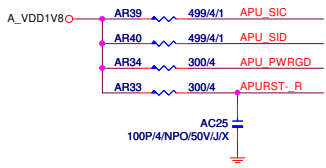


20200210_1410

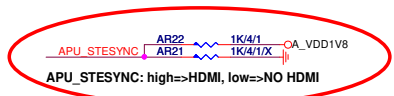
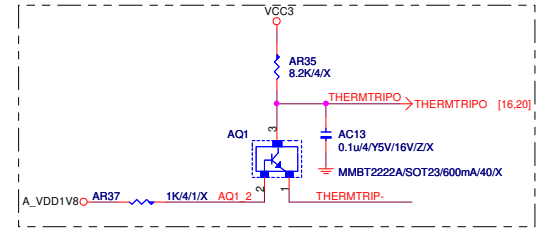
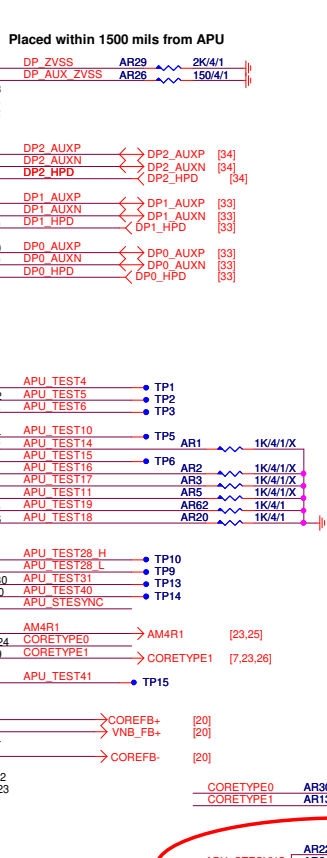
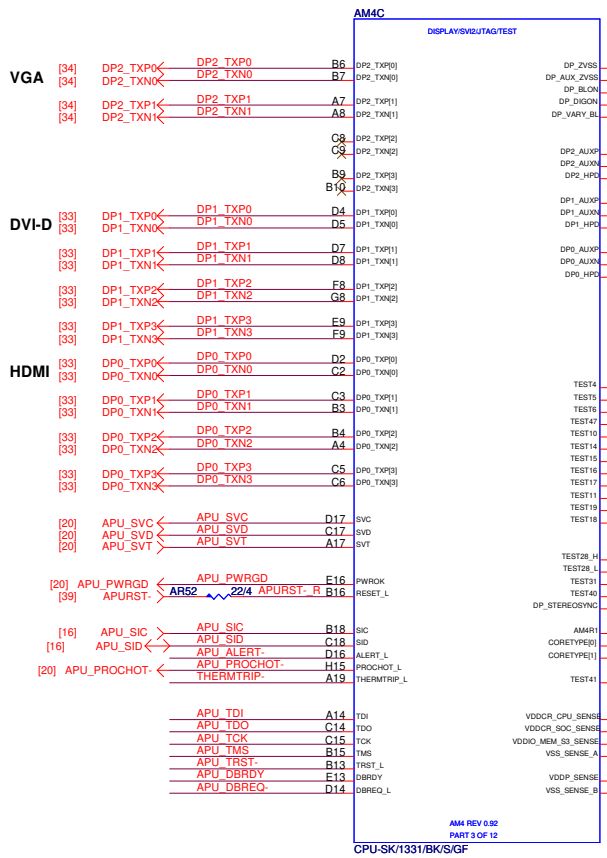
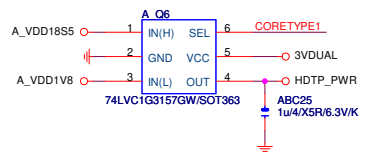
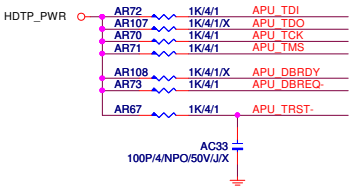
			
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Size	Document Number	Rev	
Custom	A520M H	1.0	
Date:	Monday, May 18, 2020	Sheet	1 of 39

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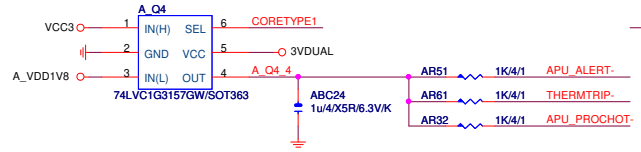




SVC	SVD	Boot voltage
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



APU_STESYNC: high=>HDMI, low=>NO HDMI



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CORETYPE 1	CORETYPE 0	Family / Model Numbers	AM4 APU TYPE
0 BR	0	Family 15 h / Models 60 h-6 Fh	TYPE 0
0 ST	1	Reserved	TYPE 1
1 ZP	0	Family 17 h / Models 00 h-0 Fh	TYPE 2
1 RV	1	Family 17 h / Models 10 h-1 Fh	TYPE 3

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Title: **CPU CONTROL**

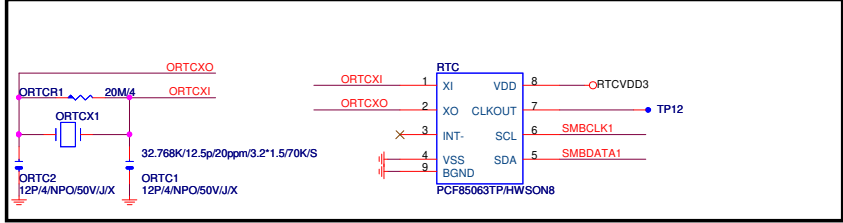
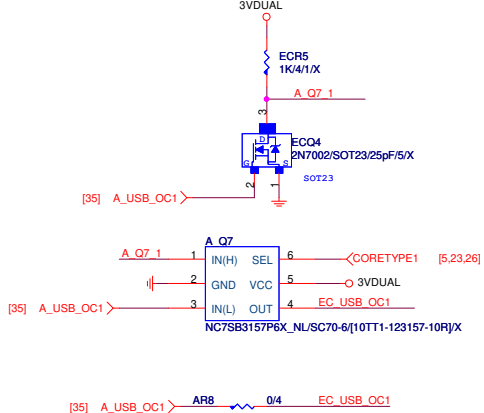
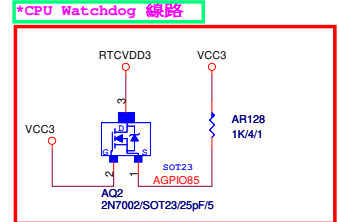
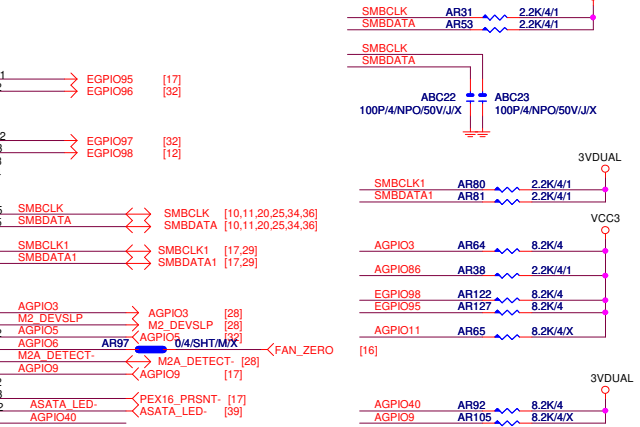
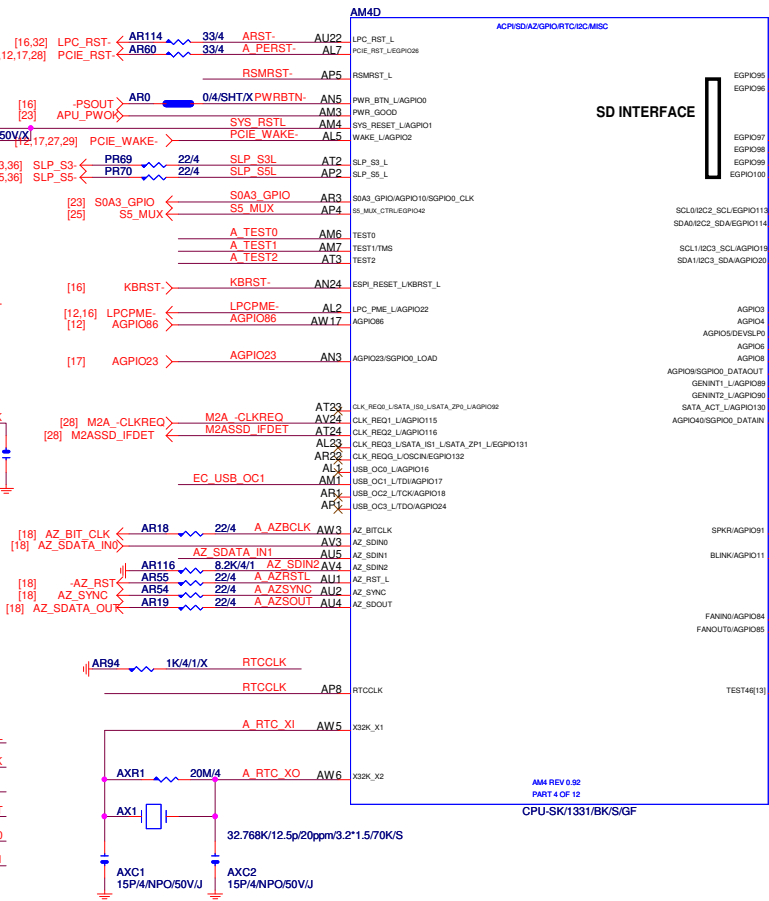
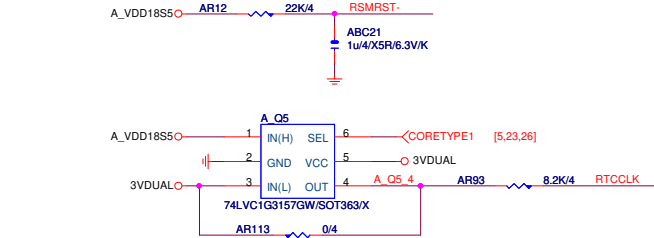
Size: Custom Document Number: **A520M H** Rev: **1.0**

Date: Friday, May 29, 2020 Sheet: 5 of 39

2	1
---	---

Internal Debug Only

TEST0	TEST1	TEST2	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.

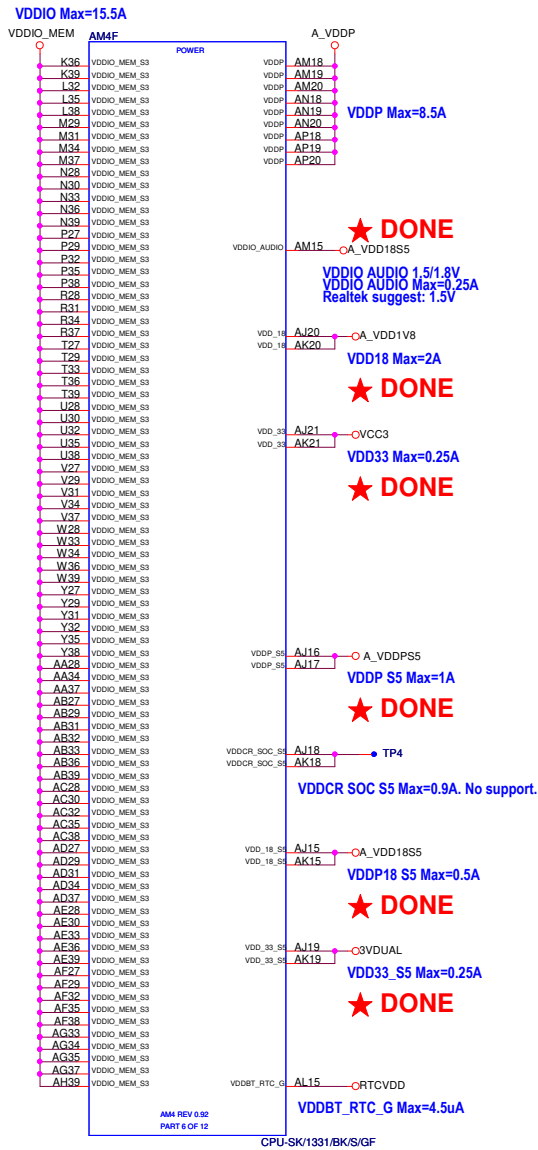


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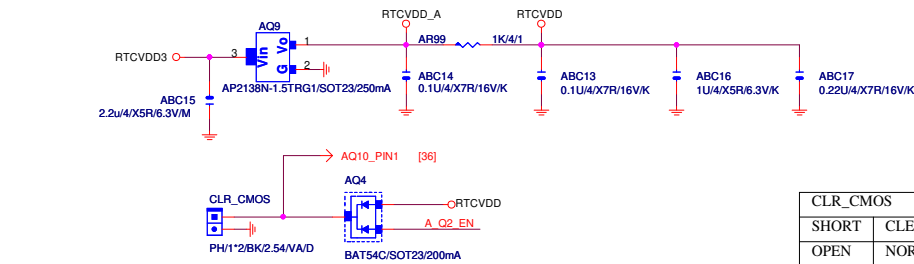
Title **AM4 MISC**

Size Custom Document Number **A520M H** Rev **1.0**

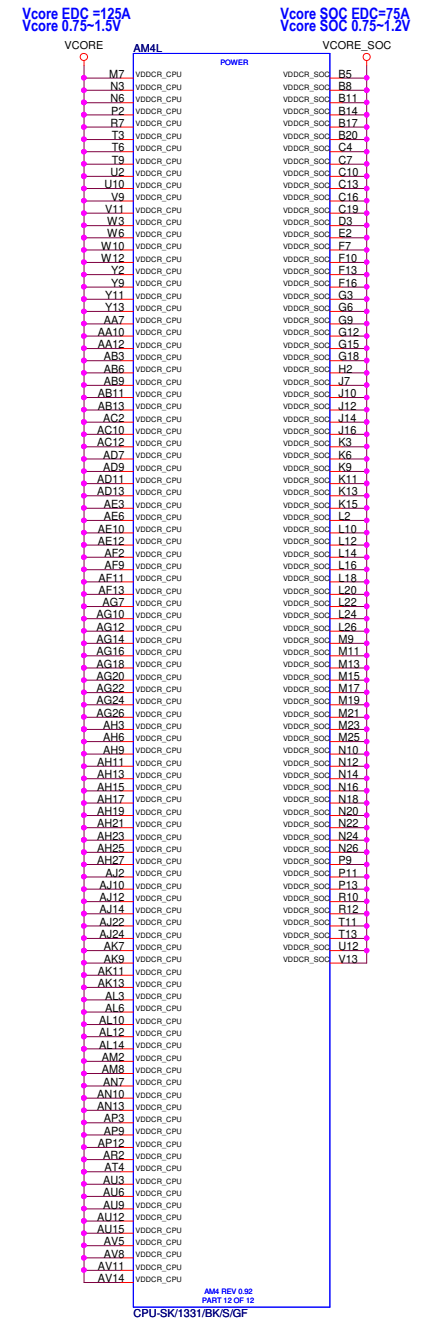
Date Monday, May 18, 2020 Sheet 7 of 39



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CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL
NOT ADD ICT FOR RTCVDD PIN	

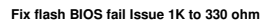


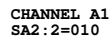
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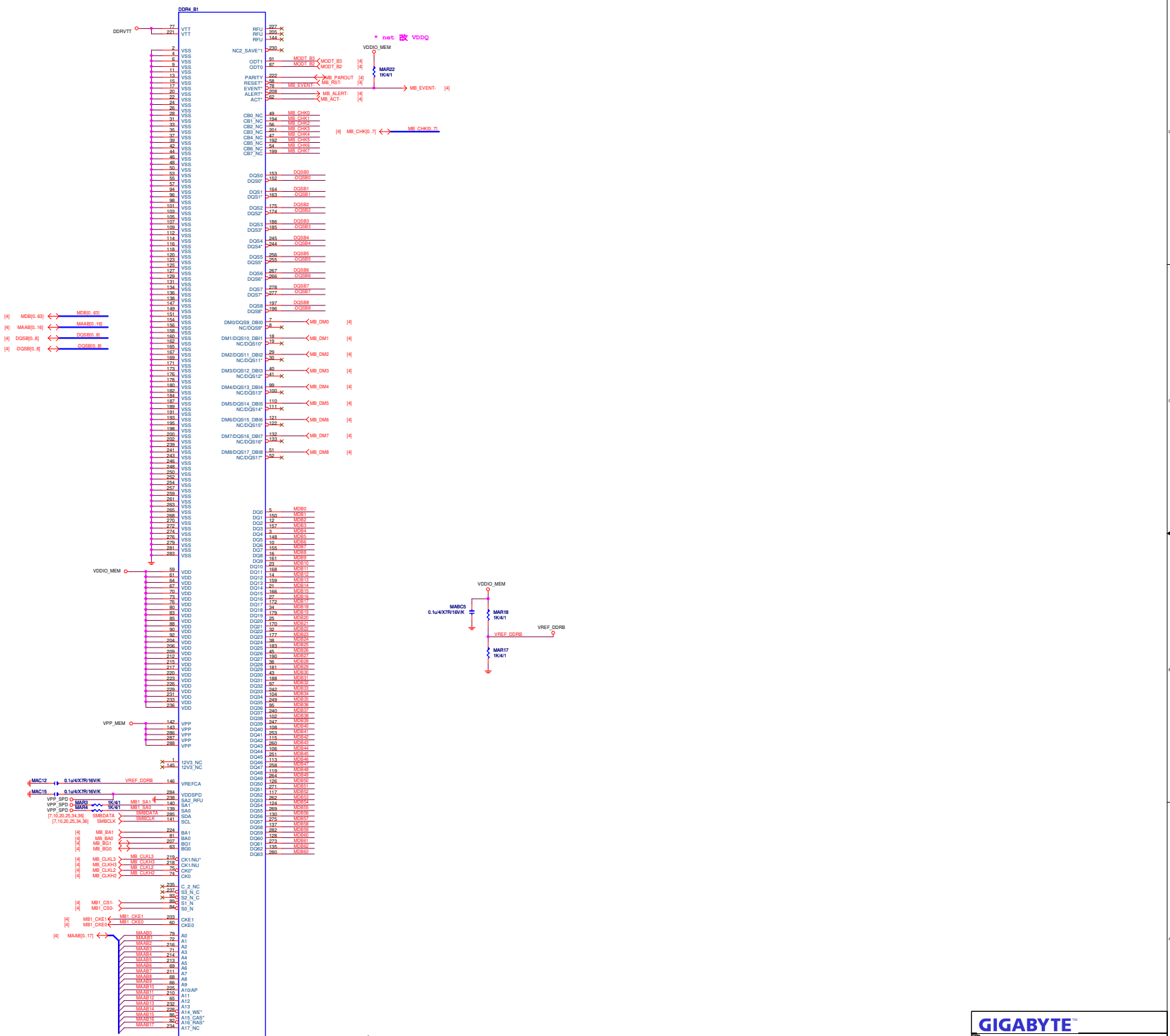
Title **CPU POWER & GND**

Size Custom Document Number **A520M H** Rev **1.0**

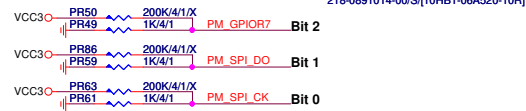
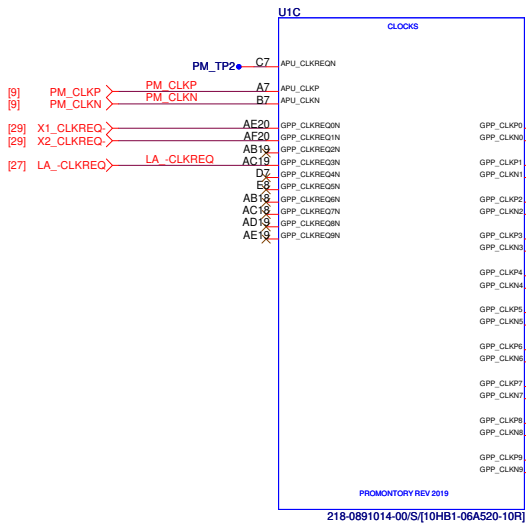
Date: Monday, May 18, 2020 Sheet 8 of 39



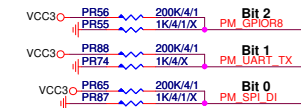




CHANNEL B1
SA2:3=011



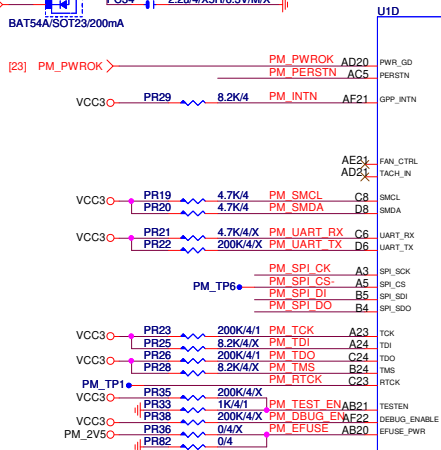
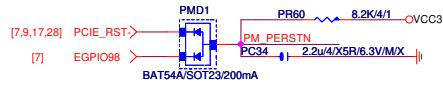
Bit 2	Bit 1	Bit 0	GPP Group 0 (Lanes 3:0)
0	0	0	4 PCIe x1
0	0	1	2 PCIe x1 + 1 PCIe x2
0	1	0	1 PCIe x2 + 2 PCIe x1
0	1	1	1 PCIe x2 + 1 PCIe x2
1	1	1	1 PCIe x4
Others: Reserved			



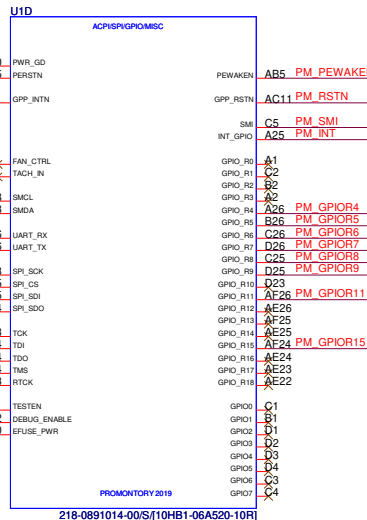
Bit 2	Bit 1	Bit 0	GPP Group 1 (Lanes 7:4)
0	0	0	4 PCIe x1
0	0	1	2 PCIe x1 + 1 PCIe x2
0	1	0	1 PCIe x2 + 2 PCIe x1
0	1	1	1 PCIe x2 + 1 PCIe x2
1	1	1	1 PCIe x4
Others: Reserved			



GPP Group 2 (Lan 8:9)=>1: PCIe x2, 0: 2 PCIe x1



TESTEN=>1:Test Mode, 0:Function mode.
DEBUG=>1:Debug Mode, 0:Function mode.



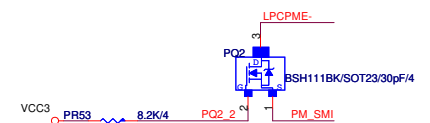
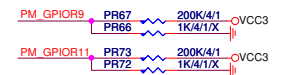
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PM_GPIOR4: GPP clock source from APU_CLKP/N;
0: GPP clock source from Crystal.

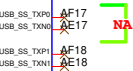
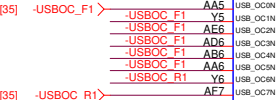
PM_GPIOR5=>1: USB3 SSC disable, 0: USB3 SSC enable

PM_GPIOR6=>1: SATA SSC disable, 0: SATA SSC enable

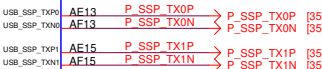
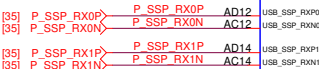


GIGABYTE ™				ANS 7990327	
Title PROMONTORY CPU/CLK/MISC					
Size	Custom	Document Number	A520M H		Rev 1.0
Date:	Wednesday, July 08, 2020	Sheet	12	of	39

USB port power control 9:0
(VCC3). Output.

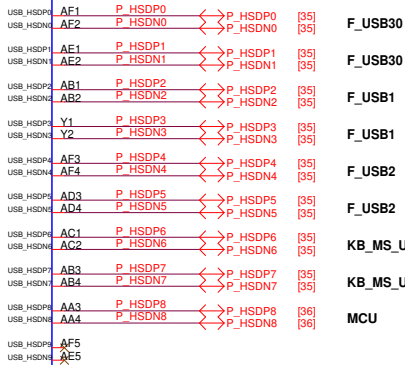


USB 3.1 Gen 2



PROMMONITORY REV 2019
218-0891014-00/S[10HB1-06A520-10R]

USB32G2	USB20	USB_OC
0	0	0
1	1	1
USB32G1		
0	2	2
1	3	3
	4	4
	5	5
	6	6
	7	7
	8	7
	9	7



F_USB30

F_USB30

F_USB1

F_USB1

F_USB2

F_USB2

KB_MS_USB

KB_MS_USB

MCU

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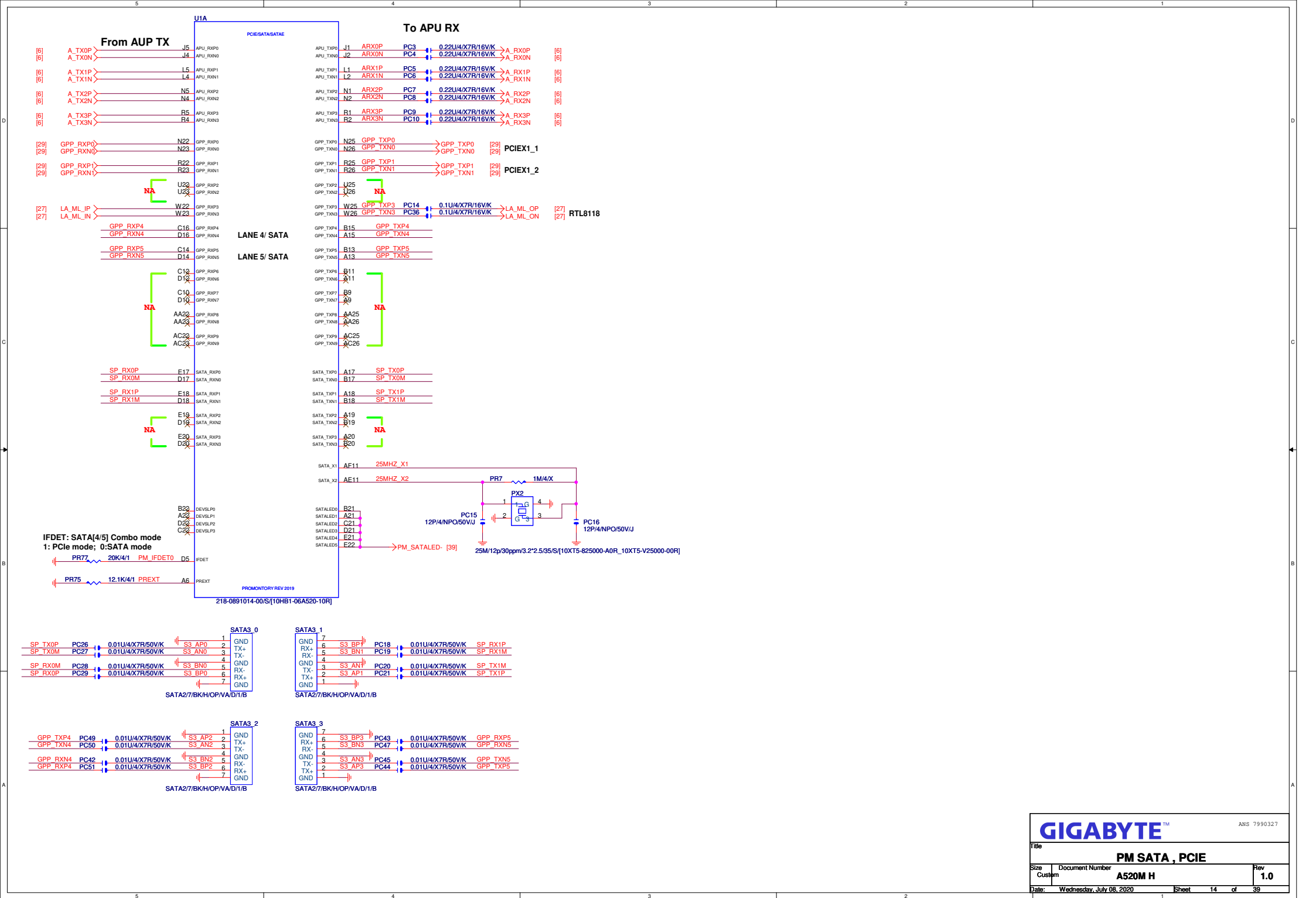
ANS 7990327

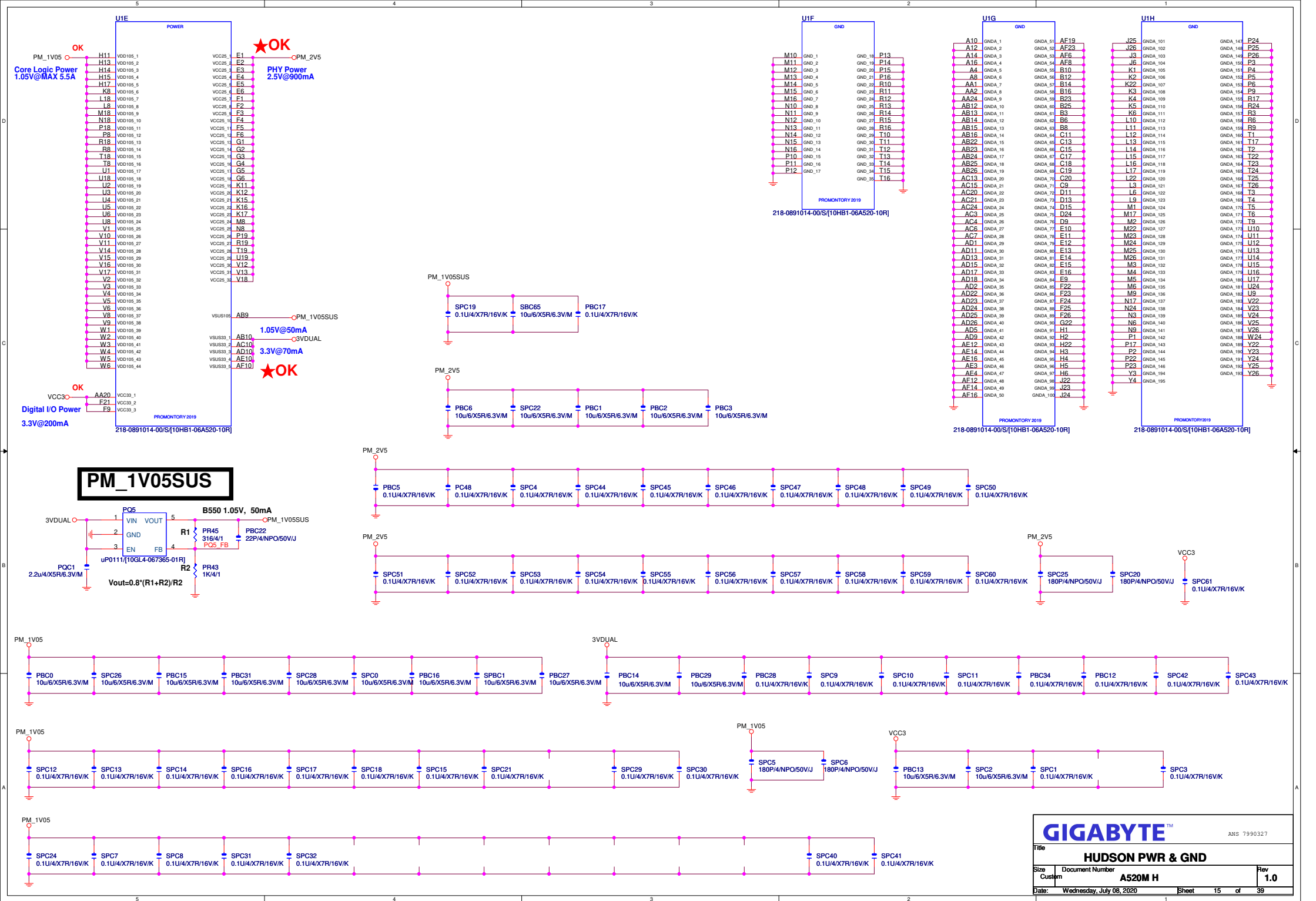
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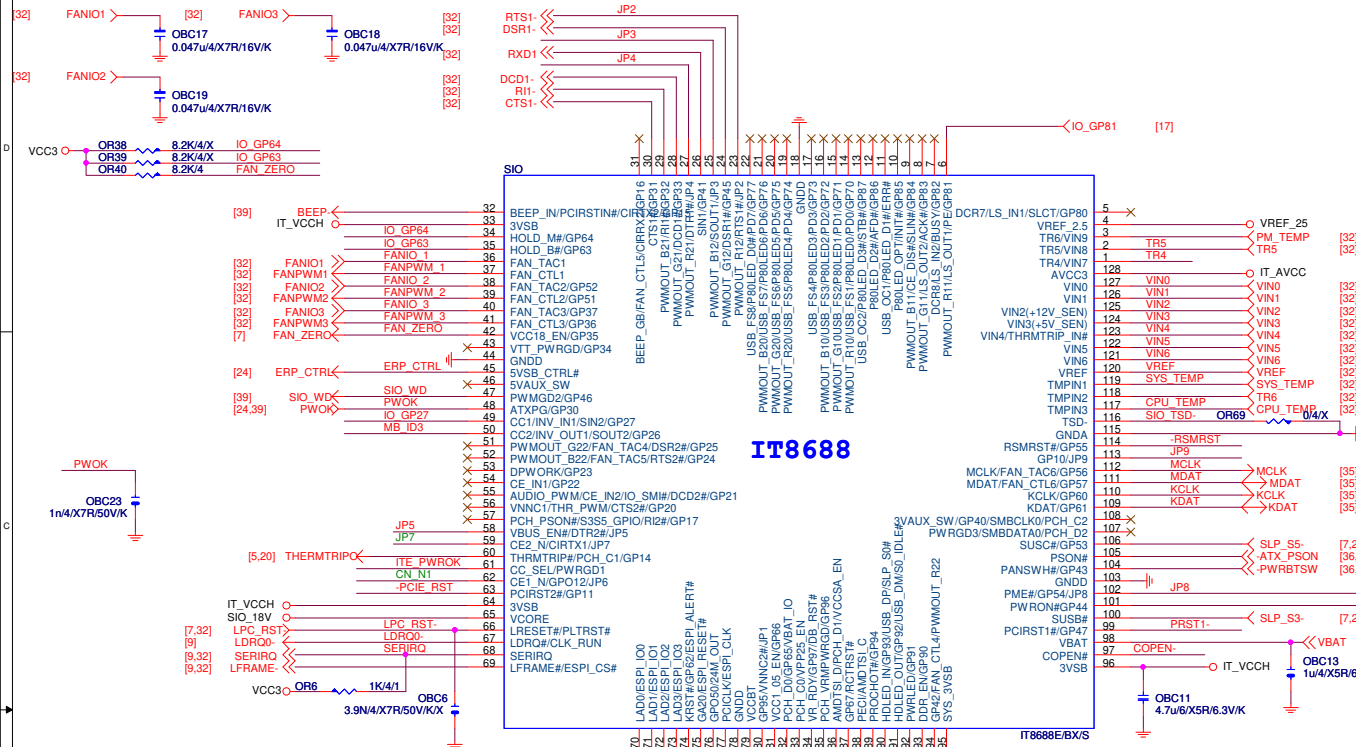
Size Custom Document Number A520M H

Rev 1.0

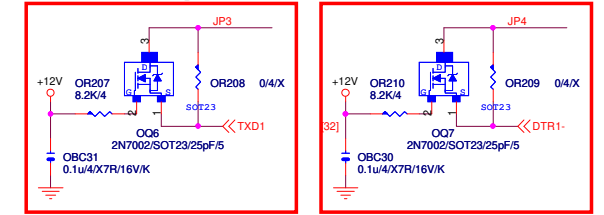
Date: Wednesday, July 08, 2020 Sheet 13 of 39



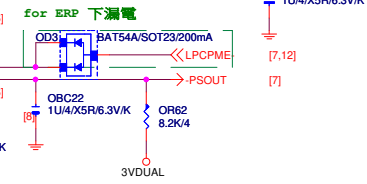
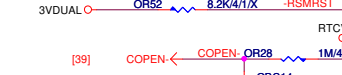




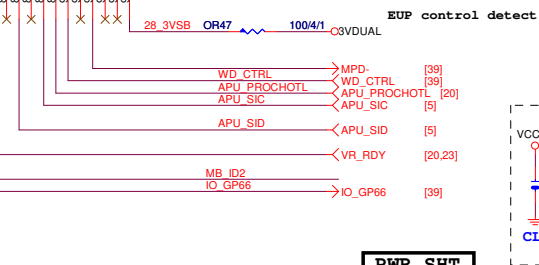
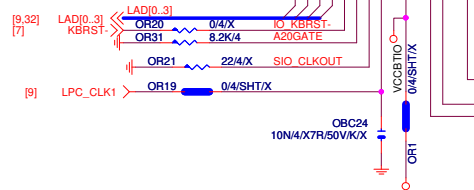
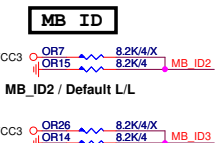
for LPC/eSPI power mode



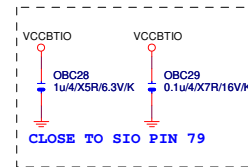
THROM SPARE GPIO



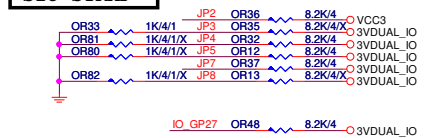
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PWR SHT

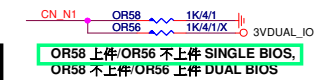


SIO STRAP

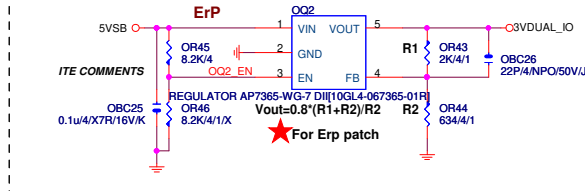
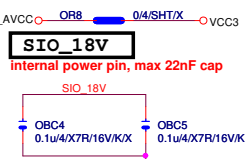


JP2	1	Disable WDT to rest PWROK
	0	Enable WDT to rest PWROK
JP3		Dual-BIOS CS pin mode select bit "0"
		See the below table
JP4	1	LPC/eSPI power VCCBT = 3.3V
	0	LPC/eSPI power VCCBT = 1.8V
JP5	1	LPC I/F
	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
	0	Disable Dual BIOS Function (for GigaByte Only)
JP7		Dual-BIOS CE pin mode select bit "1"
		See the below table
	1 1	CE pin disable (Hold pin mode)
JP7	1 0	CE mode 1
JP3	0 1	CE mode 2
	0 0	CE mode 3

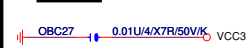
DUAL BIOS OPT STRAP



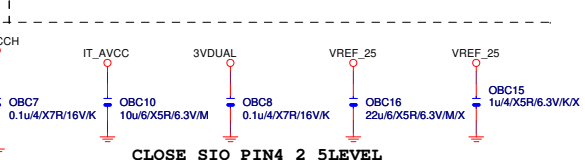
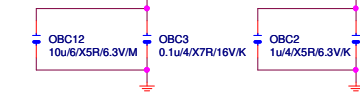
Power leakage



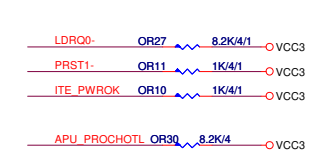
EMI



SIO CAP

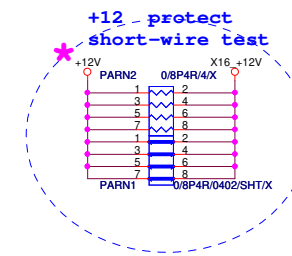
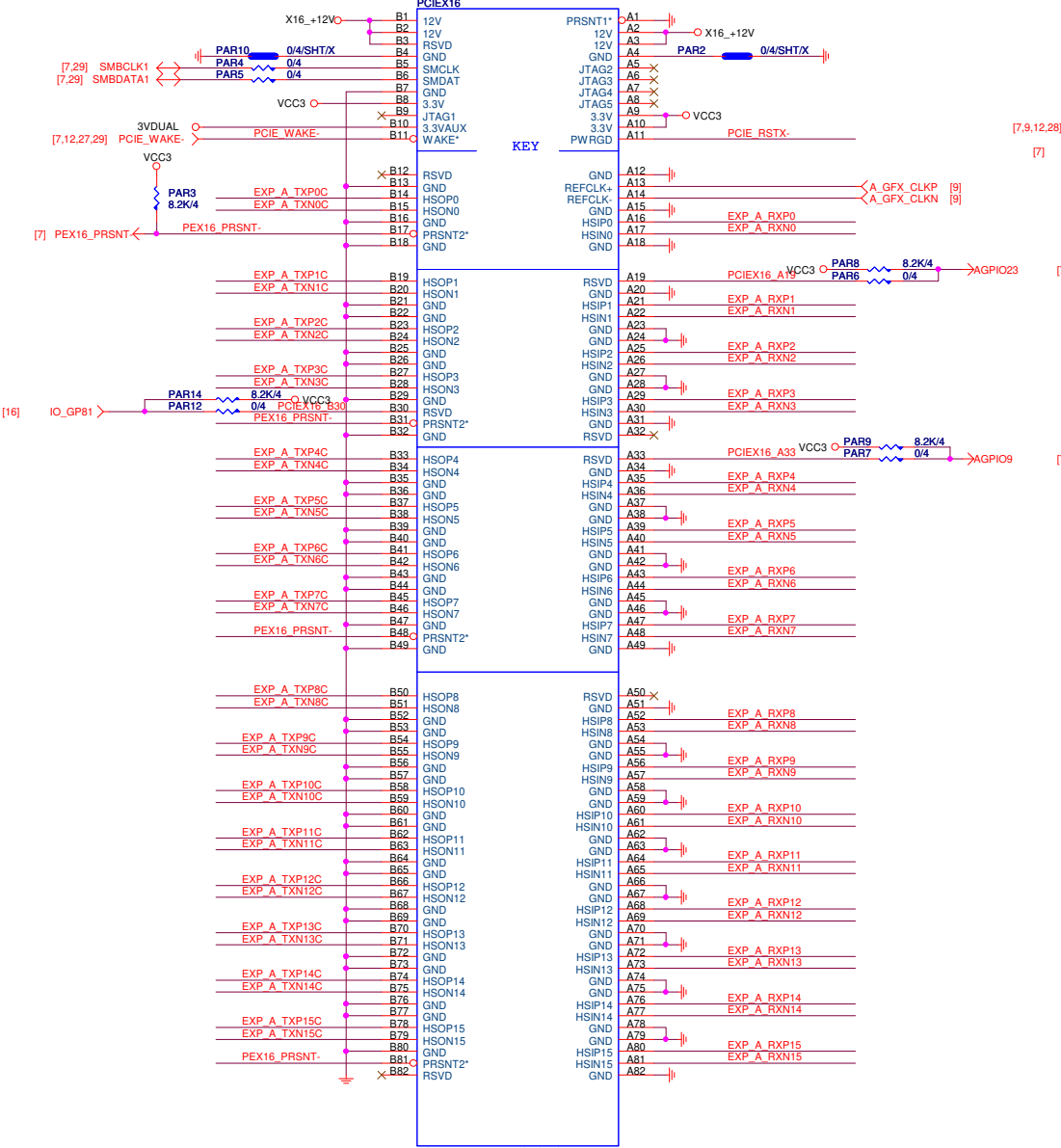


SIO PU



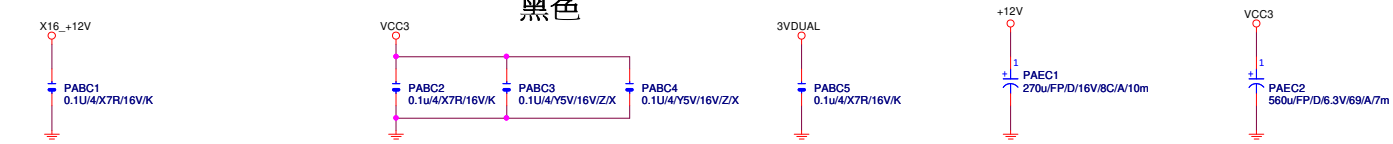
★ Footprint : PCIESLOT-164P

3GIO_*16



EXP A TXP0	PAC4	0.22u4/X5R6.3V/K	EXP A TXP0C
EXP A TXN0	PAC5	0.22u4/X5R6.3V/K	EXP A TXN0C
EXP A TXP1	PAC6	0.22u4/X5R6.3V/K	EXP A TXP1C
EXP A TXN1	PAC7	0.22u4/X5R6.3V/K	EXP A TXN1C
EXP A TXP2	PAC8	0.22u4/X5R6.3V/K	EXP A TXP2C
EXP A TXN2	PAC9	0.22u4/X5R6.3V/K	EXP A TXN2C
EXP A TXP3	PAC10	0.22u4/X5R6.3V/K	EXP A TXP3C
EXP A TXN3	PAC11	0.22u4/X5R6.3V/K	EXP A TXN3C
EXP A TXP4	PAC12	0.22u4/X5R6.3V/K	EXP A TXP4C
EXP A TXN4	PAC13	0.22u4/X5R6.3V/K	EXP A TXN4C
EXP A TXP5	PAC14	0.22u4/X5R6.3V/K	EXP A TXP5C
EXP A TXN5	PAC15	0.22u4/X5R6.3V/K	EXP A TXN5C
EXP A TXP6	PAC16	0.22u4/X5R6.3V/K	EXP A TXP6C
EXP A TXN6	PAC17	0.22u4/X5R6.3V/K	EXP A TXN6C
EXP A TXP7	PAC18	0.22u4/X5R6.3V/K	EXP A TXP7C
EXP A TXN7	PAC19	0.22u4/X5R6.3V/K	EXP A TXN7C
EXP A TXP8	PAC20	0.22u4/X5R6.3V/K	EXP A TXP8C
EXP A TXN8	PAC21	0.22u4/X5R6.3V/K	EXP A TXN8C
EXP A TXP9	PAC22	0.22u4/X5R6.3V/K	EXP A TXP9C
EXP A TXN9	PAC23	0.22u4/X5R6.3V/K	EXP A TXN9C
EXP A TXP10	PAC24	0.22u4/X5R6.3V/K	EXP A TXP10C
EXP A TXN10	PAC25	0.22u4/X5R6.3V/K	EXP A TXN10C
EXP A TXP11	PAC26	0.22u4/X5R6.3V/K	EXP A TXP11C
EXP A TXN11	PAC27	0.22u4/X5R6.3V/K	EXP A TXN11C
EXP A TXP12	PAC28	0.22u4/X5R6.3V/K	EXP A TXP12C
EXP A TXN12	PAC29	0.22u4/X5R6.3V/K	EXP A TXN12C
EXP A TXP13	PAC30	0.22u4/X5R6.3V/K	EXP A TXP13C
EXP A TXN13	PAC31	0.22u4/X5R6.3V/K	EXP A TXN13C
EXP A TXP14	PAC32	0.22u4/X5R6.3V/K	EXP A TXP14C
EXP A TXN14	PAC33	0.22u4/X5R6.3V/K	EXP A TXN14C
EXP A TXP15	PAC34	0.22u4/X5R6.3V/K	EXP A TXP15C
EXP A TXN15	PAC35	0.22u4/X5R6.3V/K	EXP A TXN15C

EXP A RXP[0..15] >> EXP_A_RXP[0..15] [6]
EXP A RXN[0..15] >> EXP_A_RXN[0..15] [6]
EXP A TXP[0..15] >> EXP_A_TXP[0..15] [6]
EXP A TXN[0..15] >> EXP_A_TXN[0..15] [6]

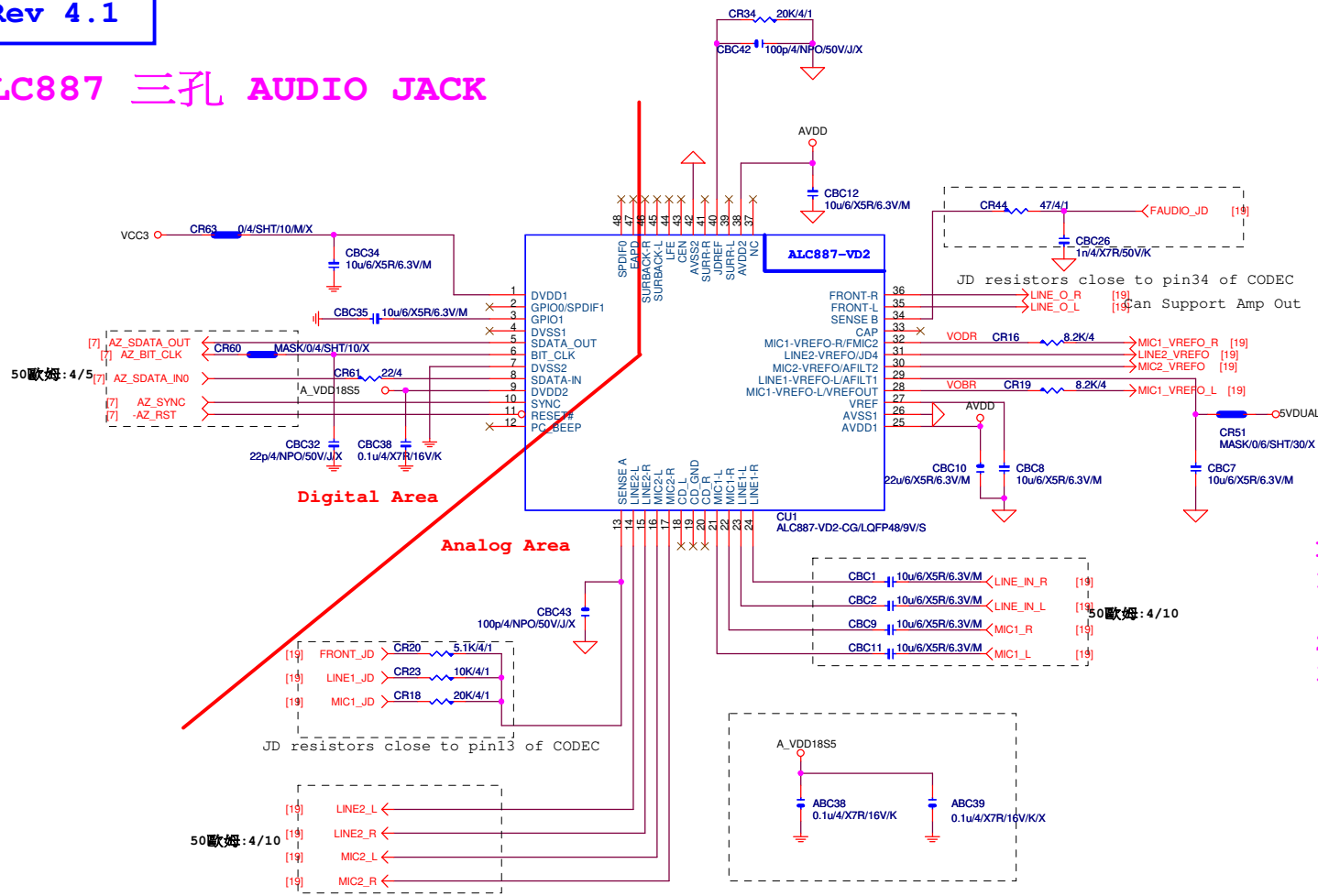


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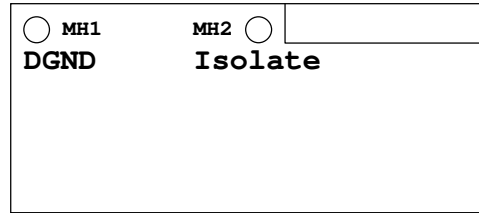
PCI EXPRESS X 16

Title	Document Number	Rev
Size	A520M H	1.0
Customer		
Date	Tuesday, May 19, 2020	Sheet 17 of 39

ALC887 三孔 AUDIO JACK

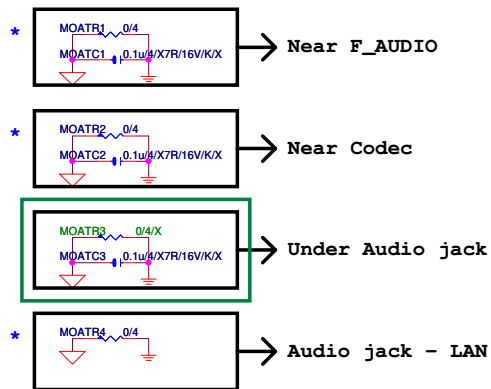


LAYOUT注意: 螺絲孔下GND方式
1. MH1空間夠, 下DGND
空間不夠, 才改為Isolate
2. MH2一律改為Isolate
3. Codec下方, 第二層必須參考GND



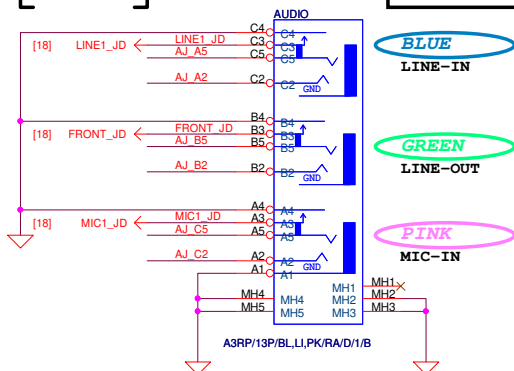
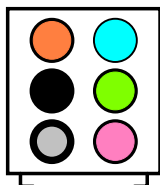
BOM OPTION : 1. Chemicon音效電容
2. 金屬外罩 Reserve (LAYOUT上件與否, 依照各Model spec)
3. LED Reserve (上件與否和LED顏色, 依照各Model spec)

Rev 4.1

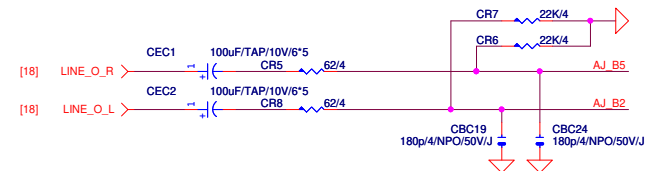


*量産前,MOATR1/MOATR2/MOATR40ohm改short pad

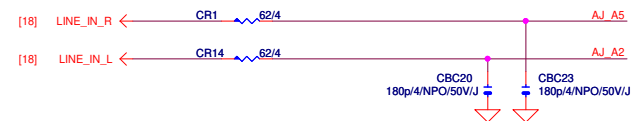
AZALIA JACK



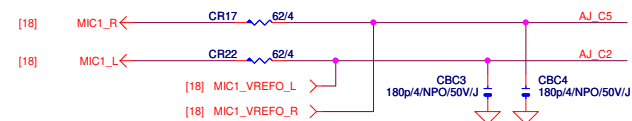
LINE-OUT



LINE-IN



MIC-IN

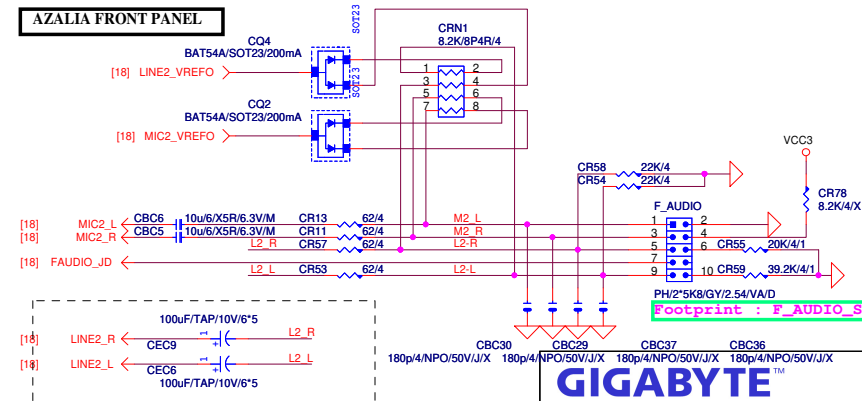


SURROUND

CEN/LFE

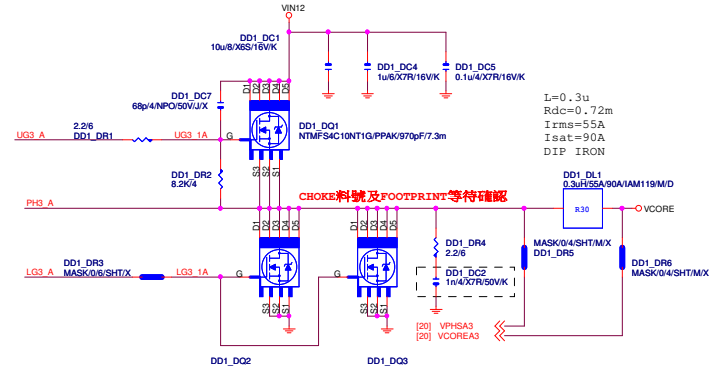
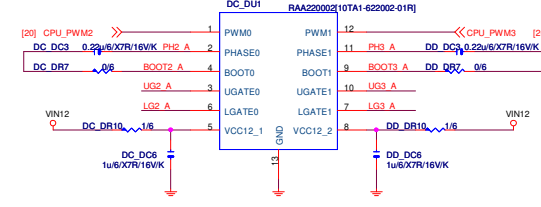
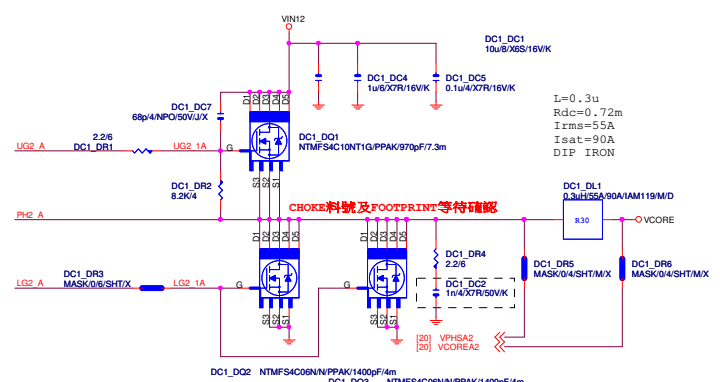
SURR BACK

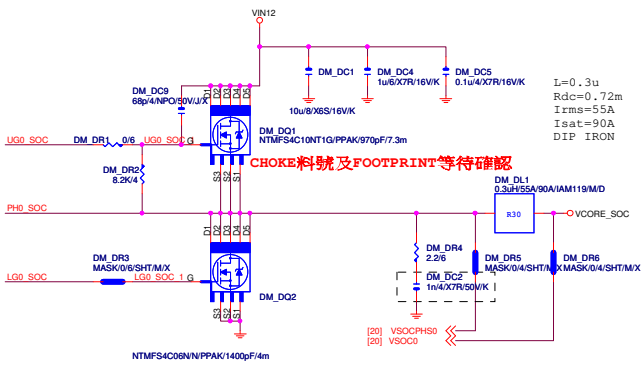
AZALIA FRONT PANEL



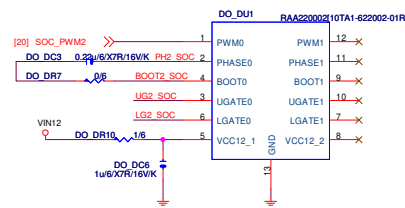
GIGABYTE

Title		
AUDIO JACK		
Size	Document Number	Rev
Custom	A520M H	1.0
Date:	Monday, May 18, 2020	Sheet 19 of 39

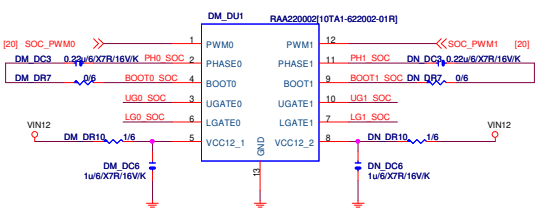




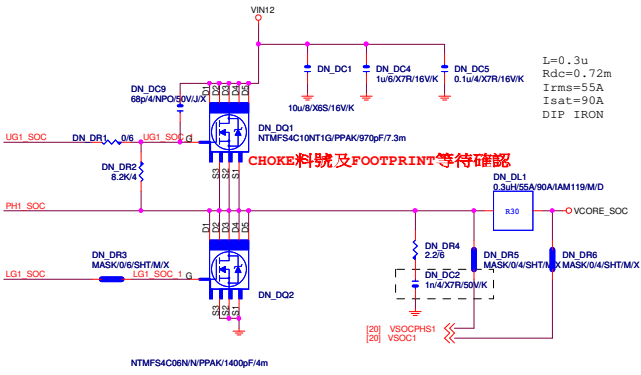
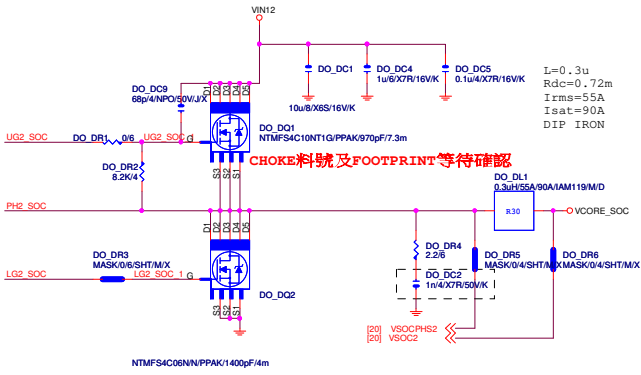
CHOKE料號及FOOTPRINT等待確認



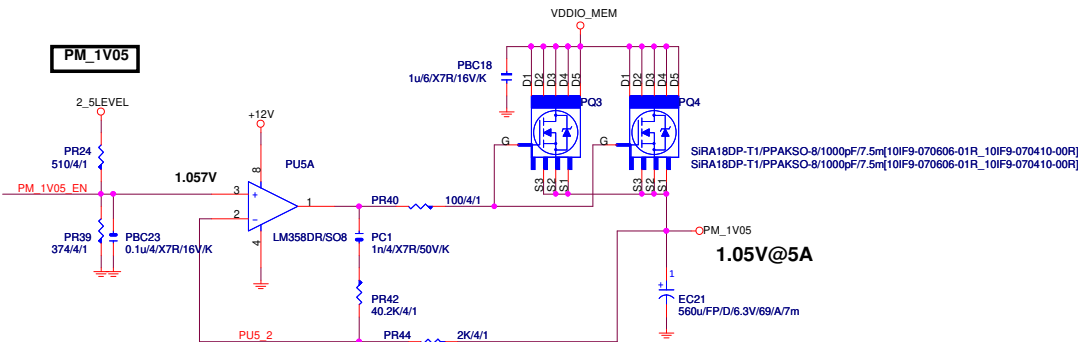
CHOKE料號及FOOTPRINT等待確認



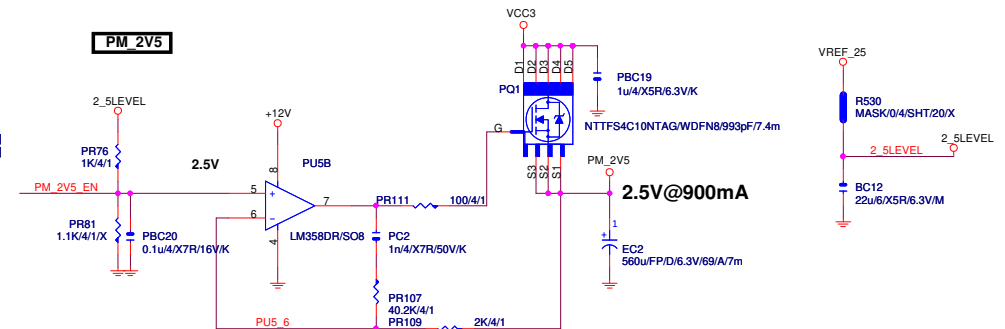
CHOKE料號及FOOTPRINT等待確認



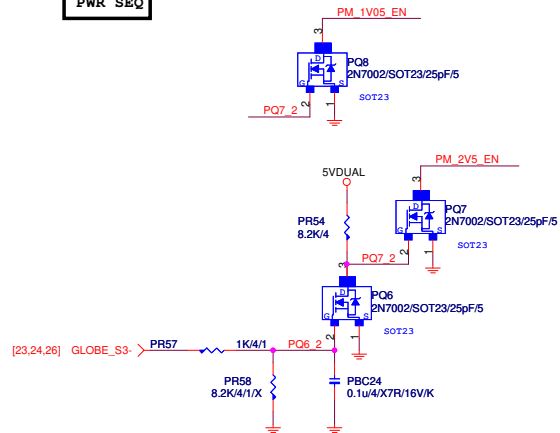
PM_1V05



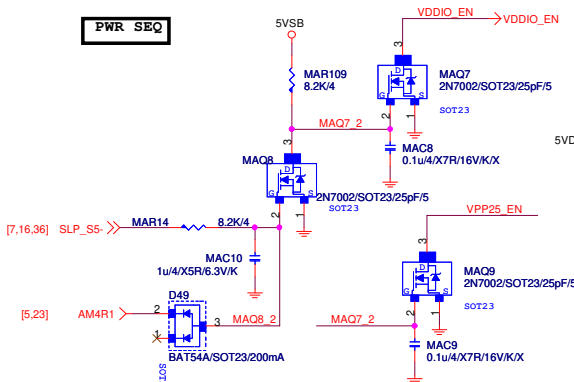
PM_2V5



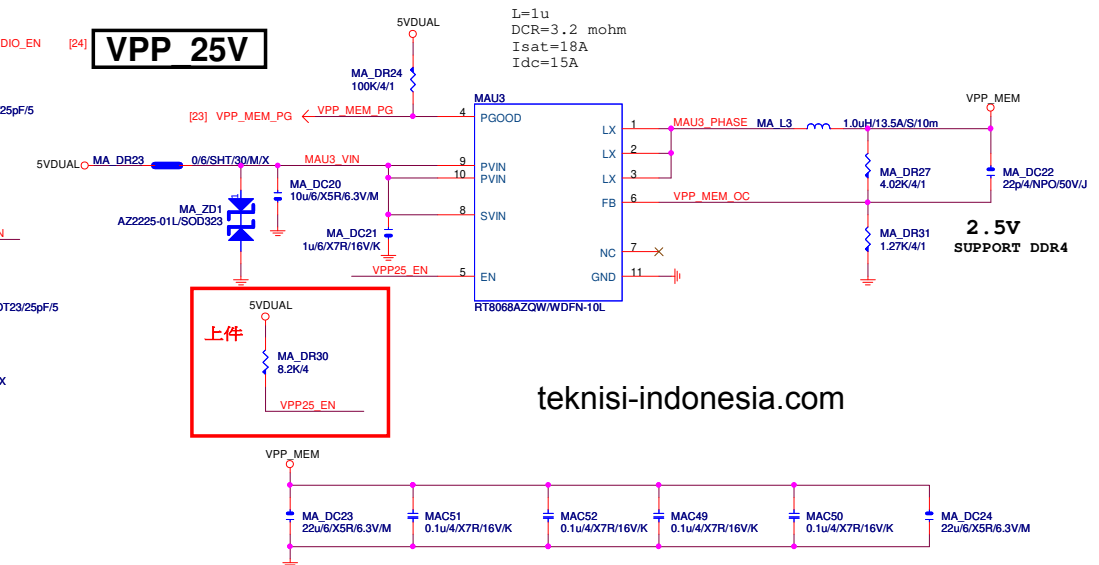
PWR_SEQ



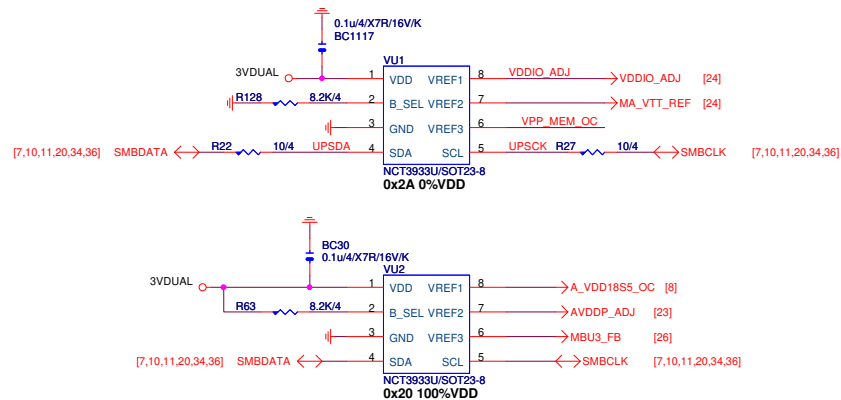
PWR_SEQ



VPP 25V



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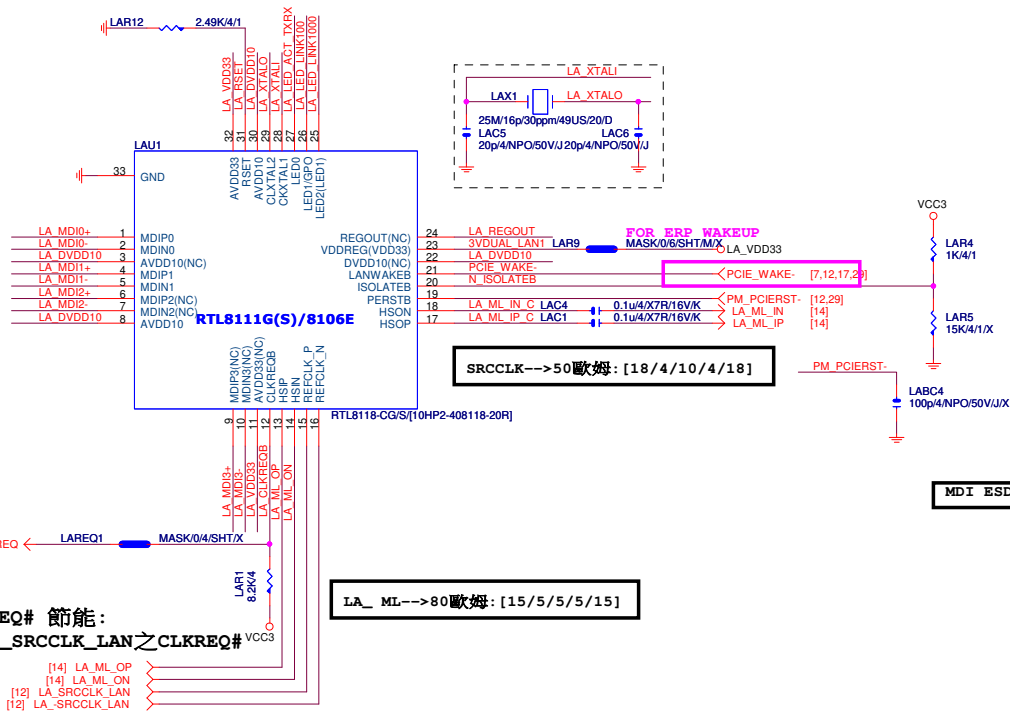


Address	0x2A	0x28	0x26	0x24	0x22	0x20
R1 (kΩ)	open	3.9	3	2.2	1.3	10
R2 (kΩ)	10	1.3	2.2	3	3.9	open
ADD_SEL Voltage (% of VCC)	0	25	42	58	75	100

Table1. Recommended Slave Address Setting

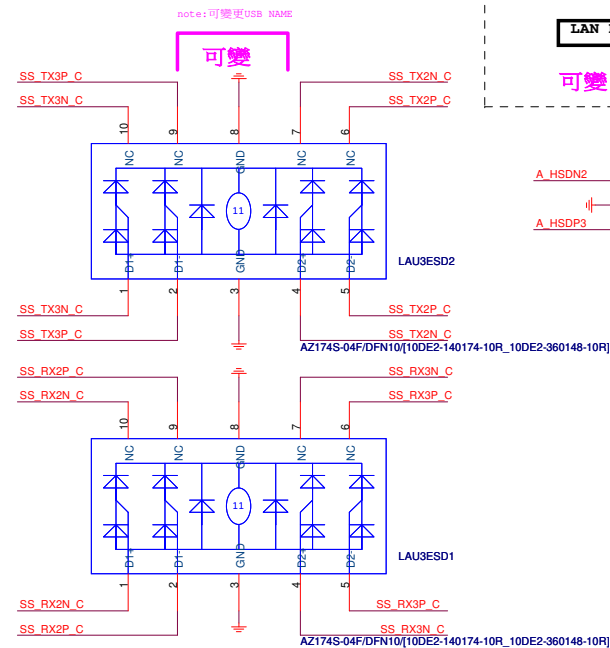
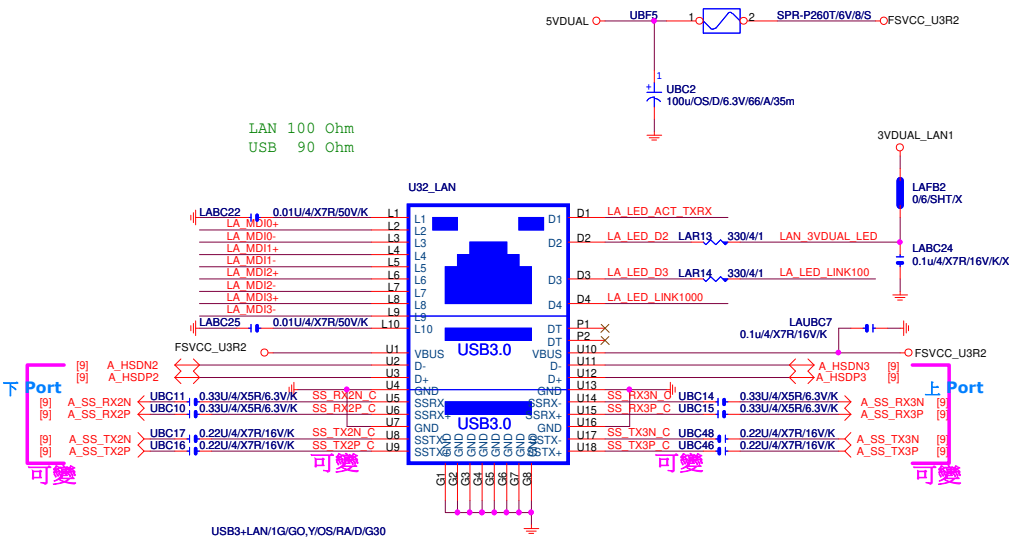
GIGABYTE

Title		PM POWER		Rev	1.0
Size	Document Number	A520M H			
Date:	Monday, May 18, 2020	Sheet	25	of 39	

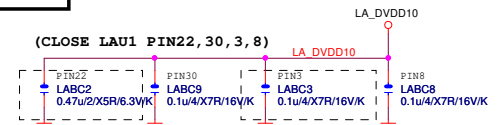


USB_LAN CONNECTOR

note:可變更USB NAME



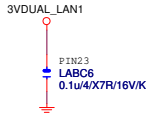
LAN POWER



```
LABC2:1U CLOSE PIN22 [REALTEK REQ]
```

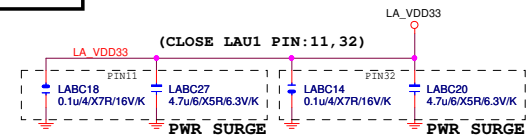
LAN POWER

note: lan power連接及電流



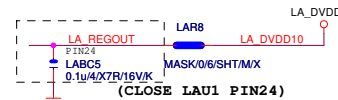
(CLOSE LAU1 PIN23)

LAN POWER



```
LABC18,27:CLOSE PIN11[REALTEK SURGE]
LABC14,20:CLOSE PIN32[REALTEK SURGE]
```

LAN POWER

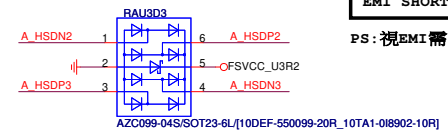


LAN POWER

note: lan power連接及電流

For PVT :LAPW1 改 R0402-2-SHORT20

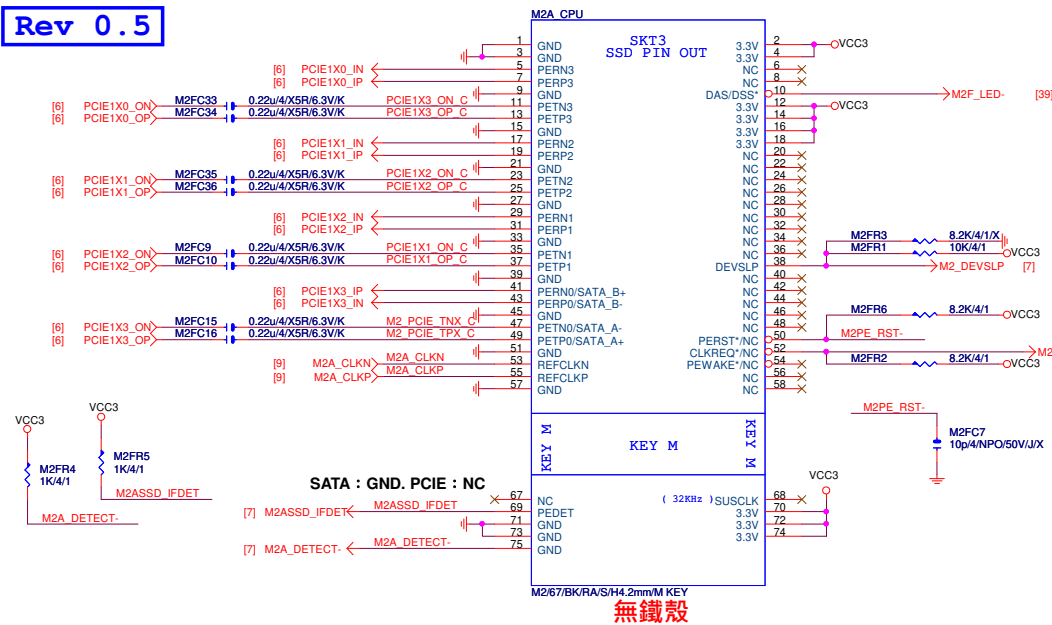
可變



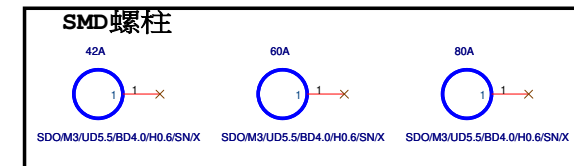
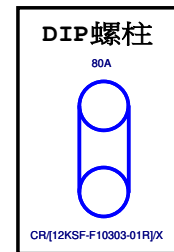
EMI SHORT PAD

PS:視EMI需求

Rev 0.5

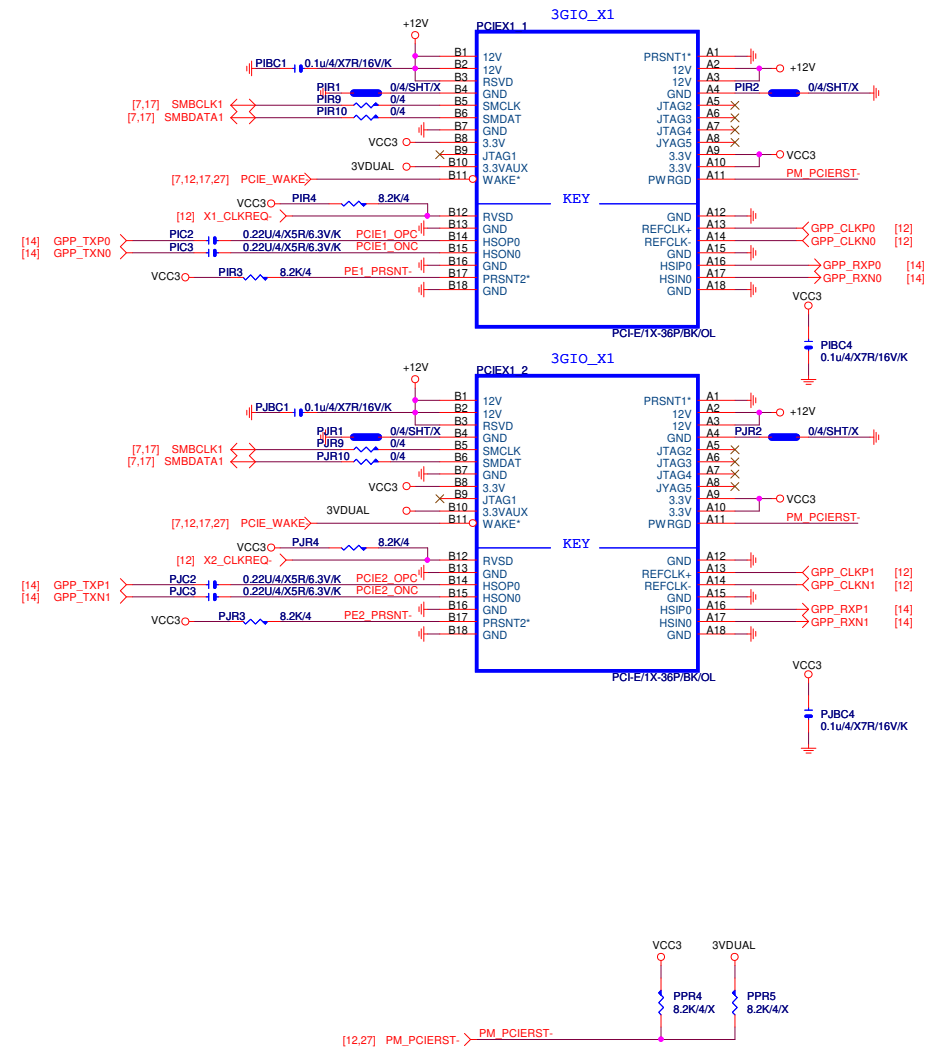


Footprint : NGFF-M-75P-8CM-09MM-SMD



★ Footprint : HOLE_165NP for 塑膠扣具

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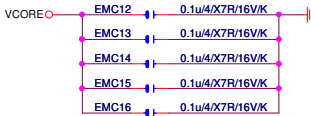
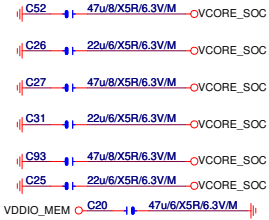
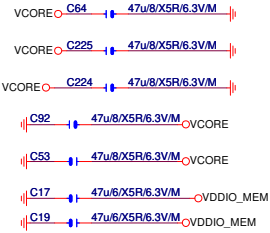
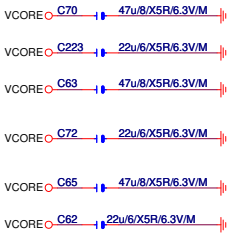
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Title **PCIE X4, X1**

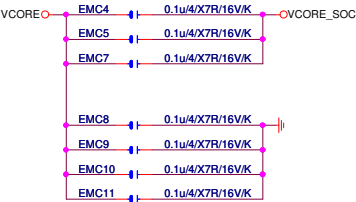
Size Custom Document Number **A520M H** Rev **1.0**

Date: Monday, May 18, 2020 Sheet 29 of 39

CPU TOP CAVITY



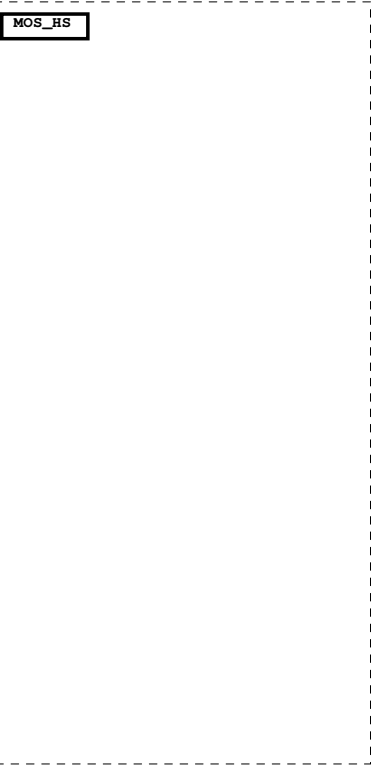
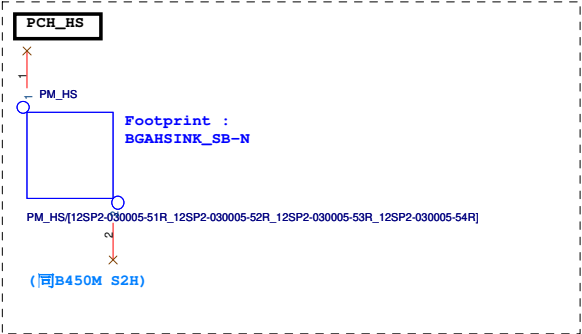
Cross Plane CAP



Cross Plane CAP



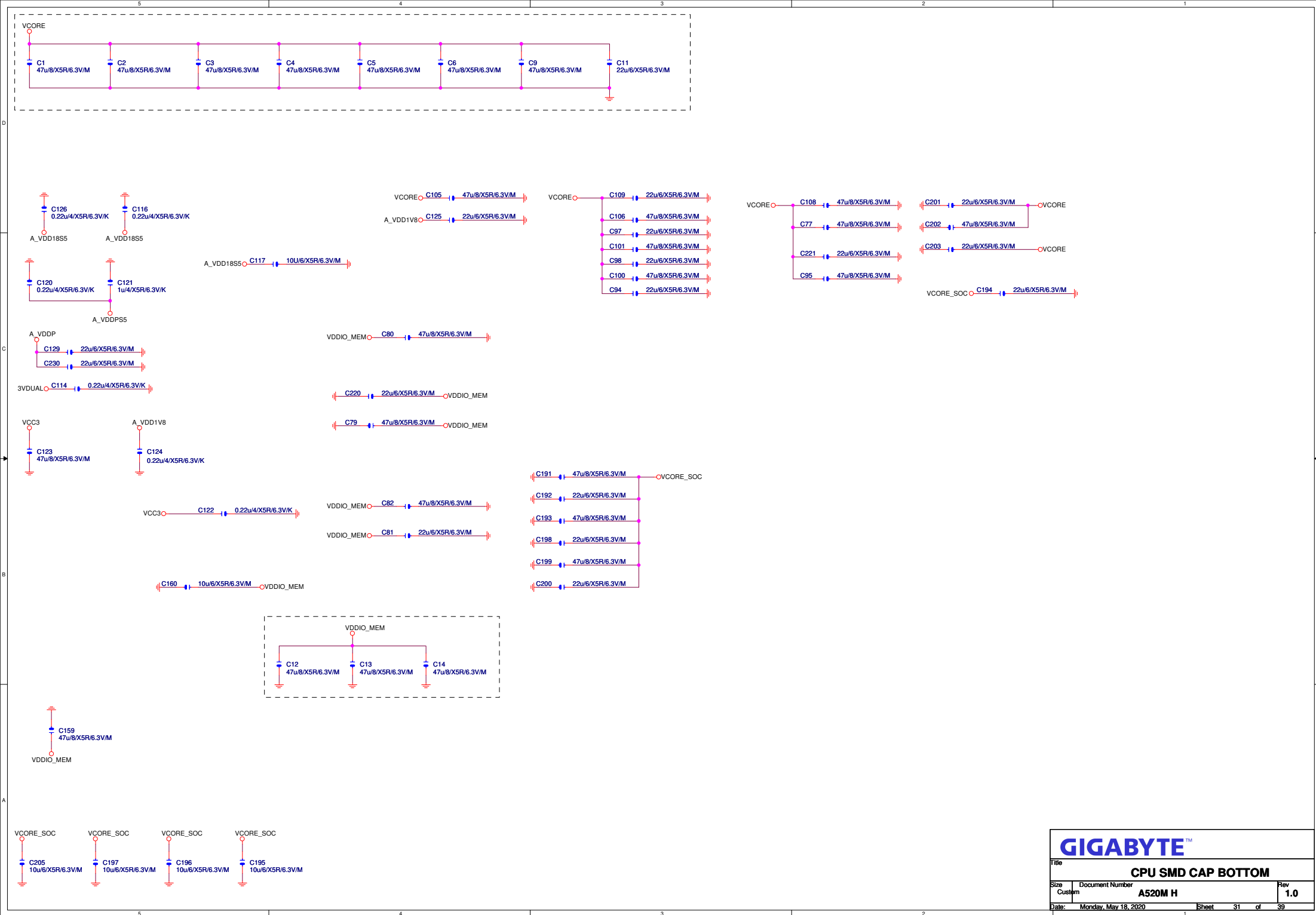
裝甲HEATSINK 分成五大部份



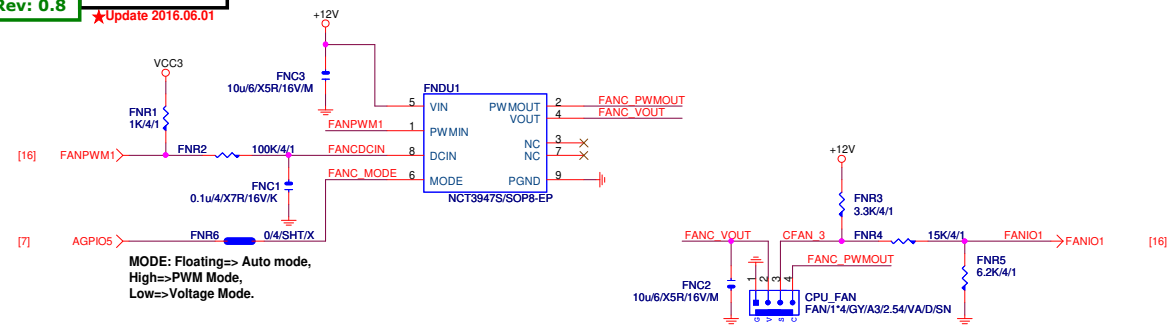
- * PCB顏色 : 咖啡黑
- * 文字面 : 灰色
- * 圖騰 : 同B450M S2H

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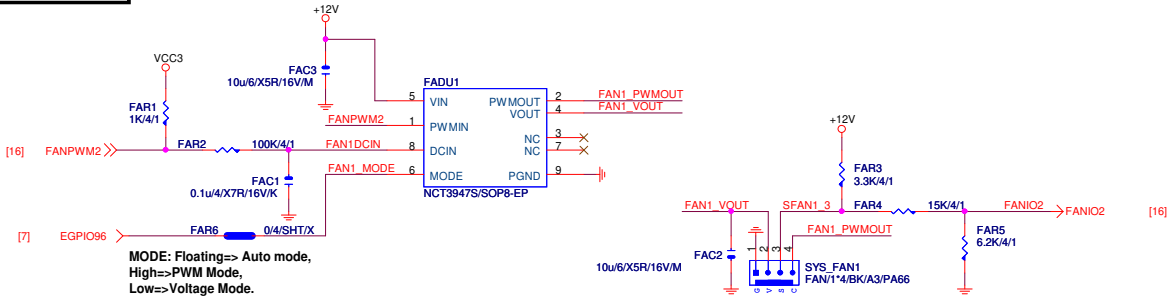
Title			CPU TOP CAP	
Size	Document Number	A520M H		Rev 1.0
Date:	Monday, May 18, 2020	Sheet	30	of 39



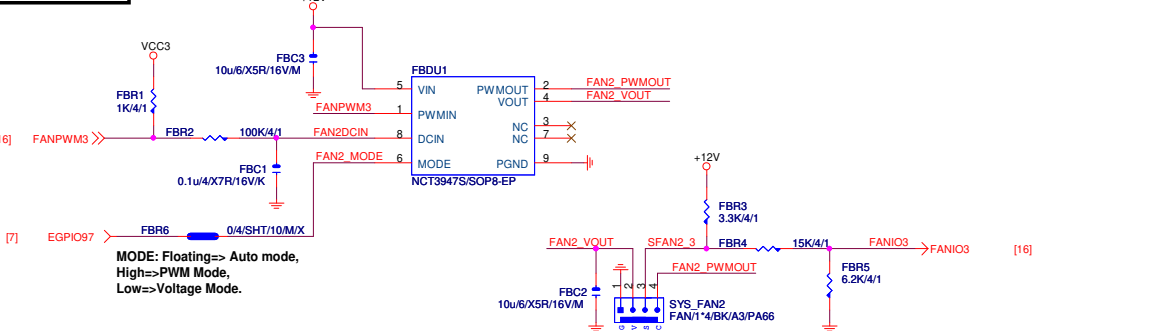
★Update 2016.06.01



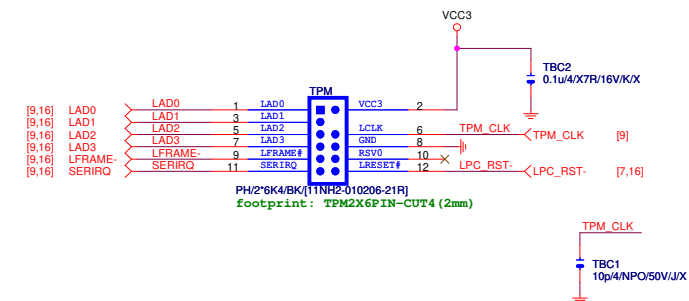
SYSTEM FAN1



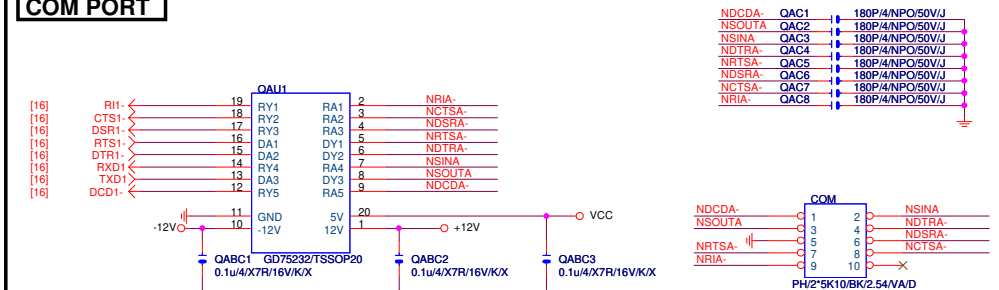
SYSTEM FAN2



TPM



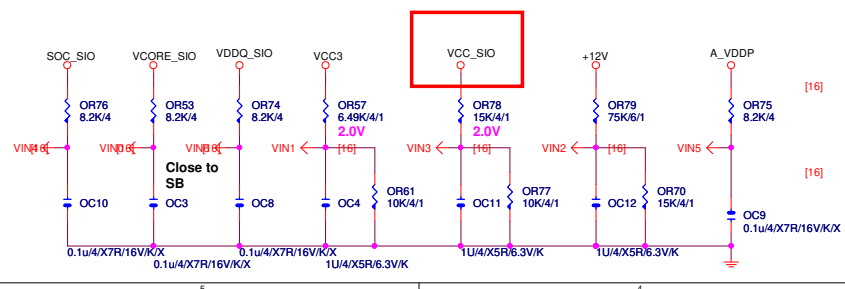
COM PORT



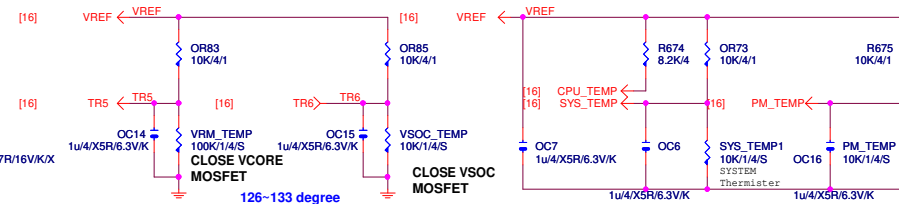
LPT PORT

Hardware Monitor circuits - VOLTAGE

Rev: 0.6

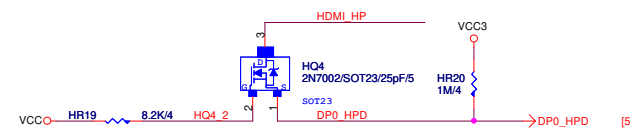
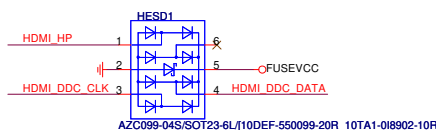
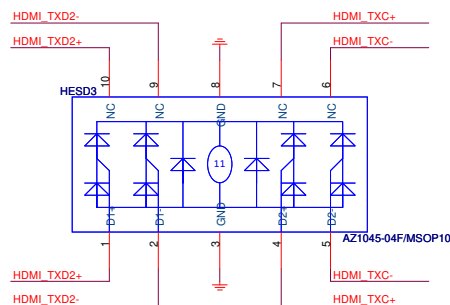
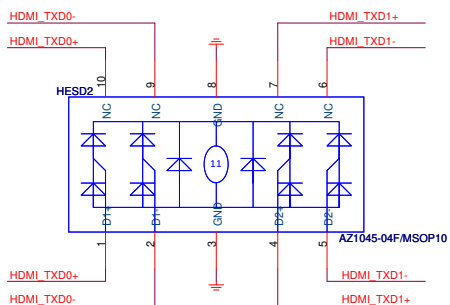
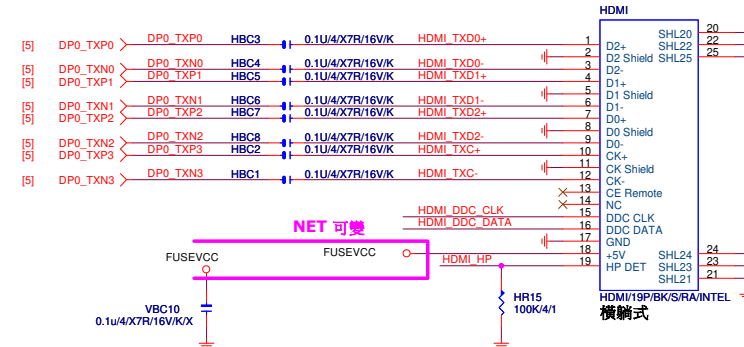
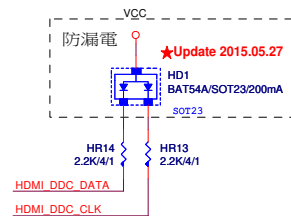
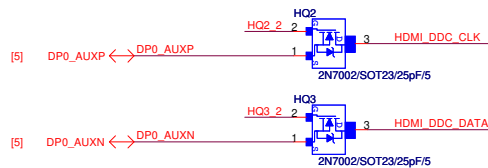
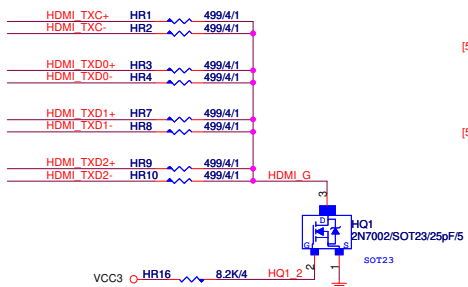


Hardware Monitor circuits - Temperature



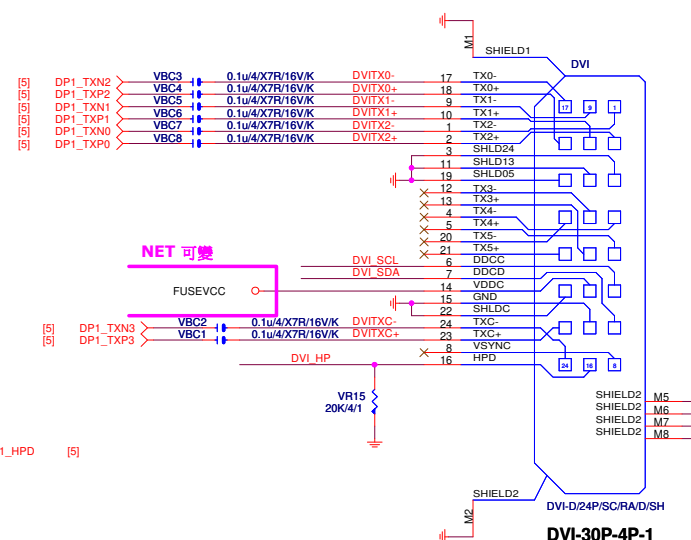
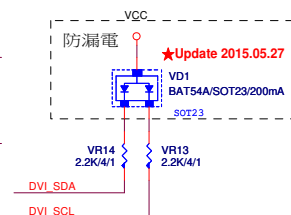
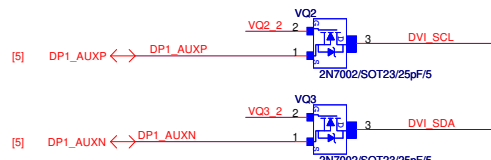
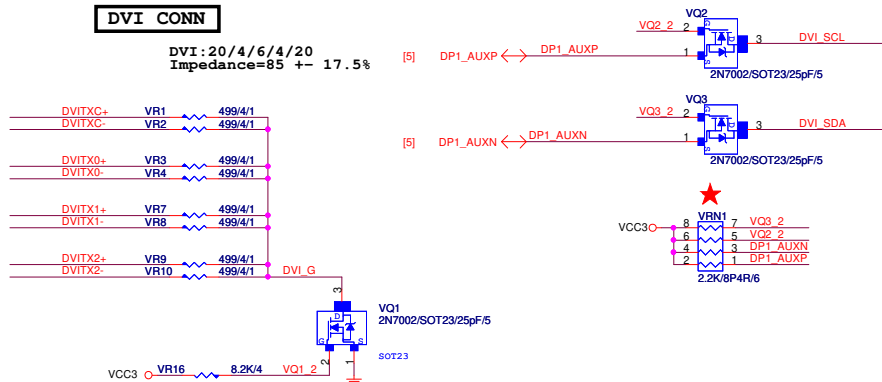
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Title			
FAN, LPT, COM ,HWM			
Size	Document Number	Rev	
Custom	A520M H	1.0	
Date:	Friday, May 22, 2020	Sheet	32 of 39

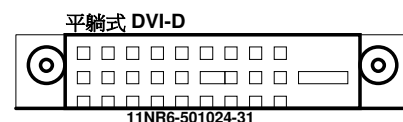
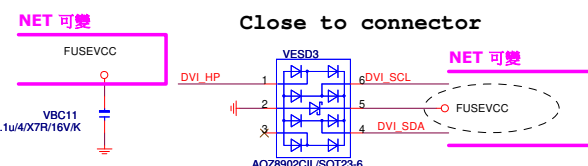
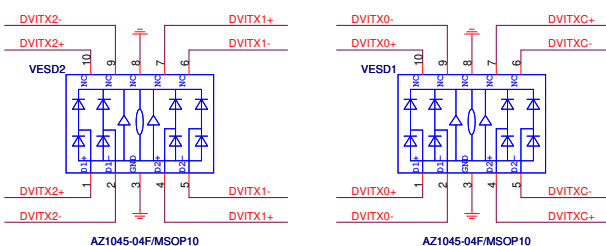


DVI CONN

DVI: 20/4/6/4/20
Impedance=85 +- 17.5%



Close to connector

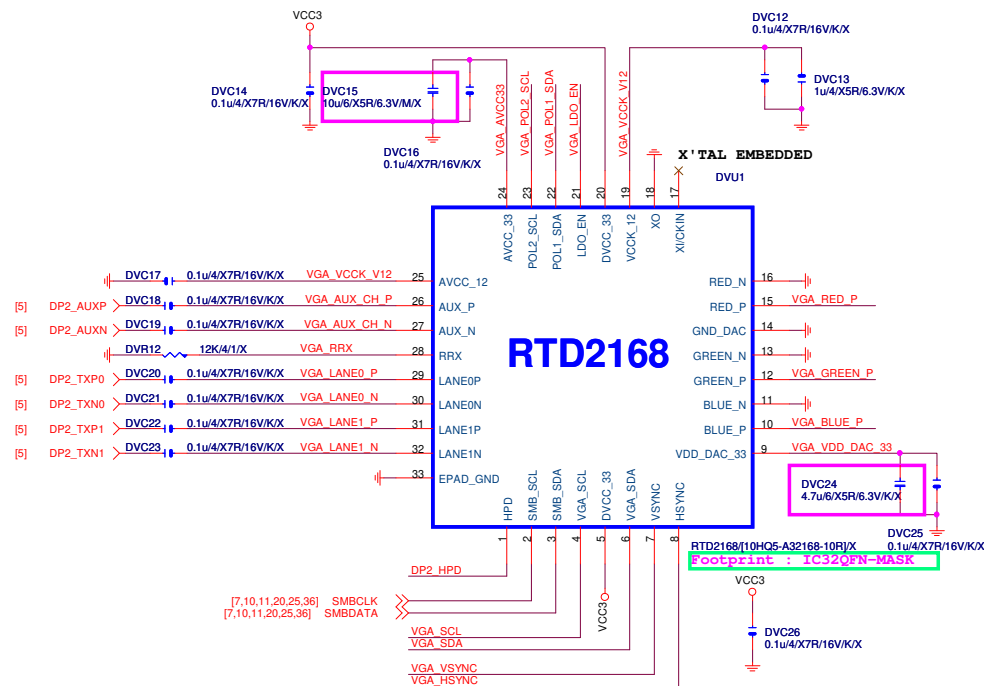


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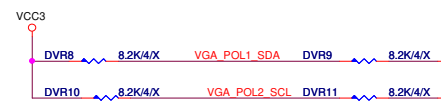
Title: **HDMI,DVI**

Size: Custom Document Number: **A520M H** Rev: **1.0**

Date: Monday, May 18, 2020 Sheet: 33 of 39



Power on latch



		POL1_SDA(PIN22)	
		0	1
POL2_SCL (PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

Embedded LDO



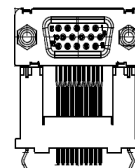
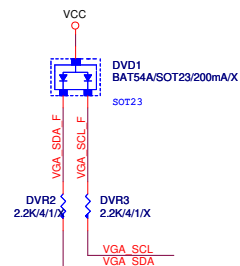
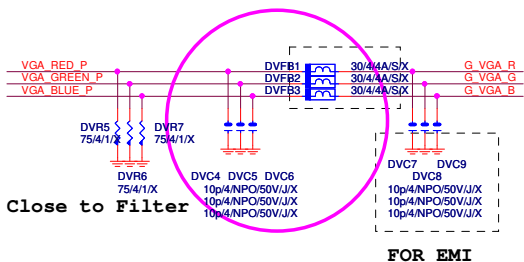
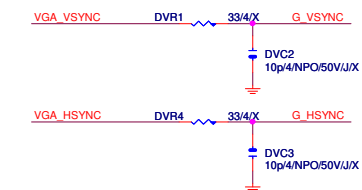
LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

DP HPD



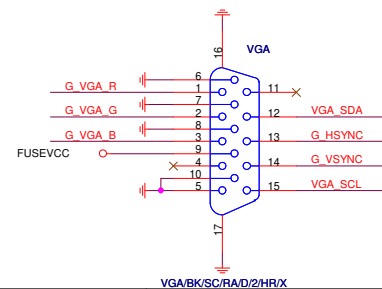
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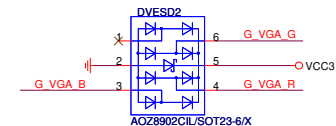
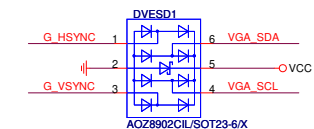


架高型VGA (BLACK)

Footprint : VGACONN-DH-2-MASK



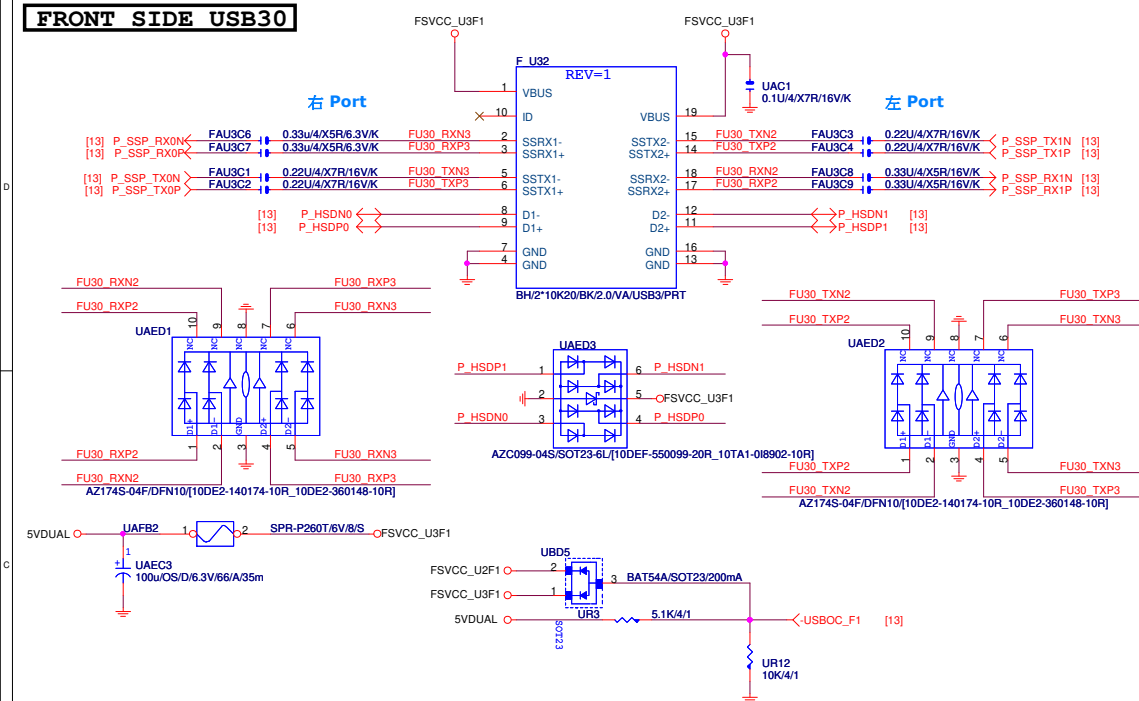
VGA ESD



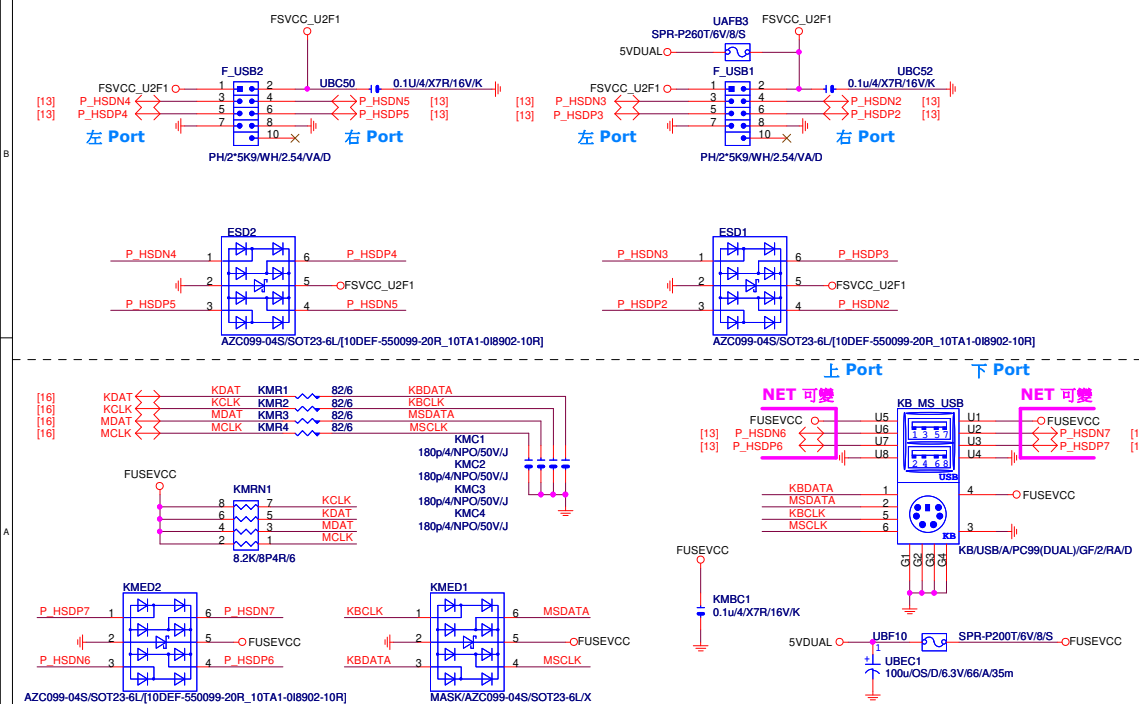
VGA

Title			
VGA			
Size	Document Number	Rev	
Custom	A520M H	1.0	
Date:	Monday, May 18, 2020	Sheet	34 of 39

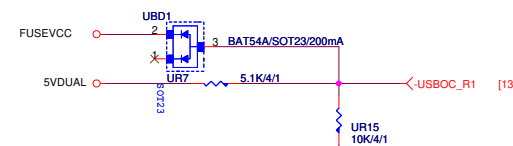
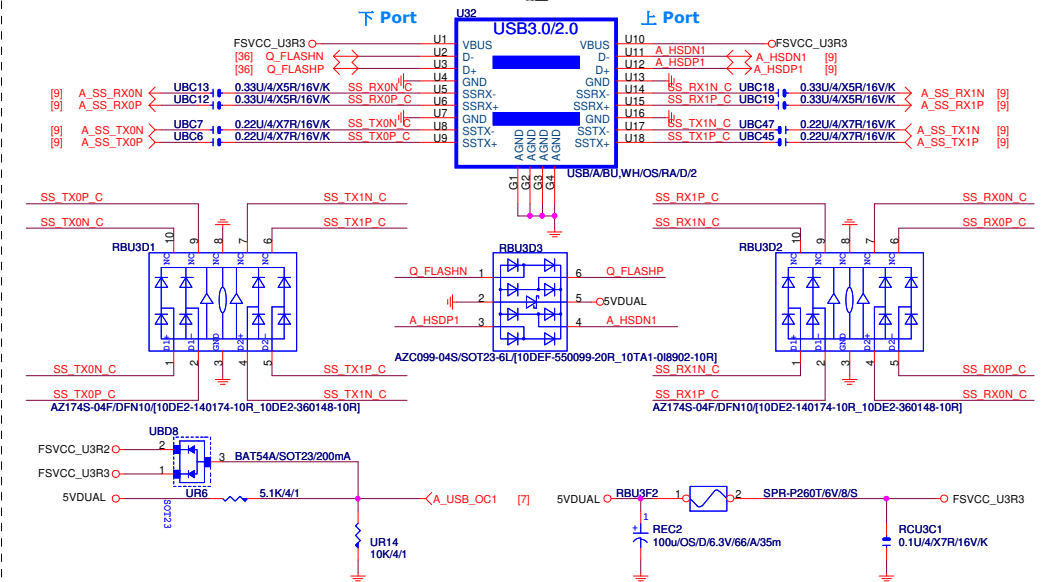
FRONT SIDE USB30

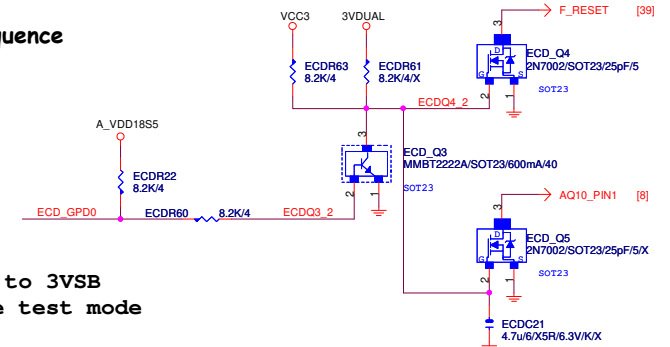
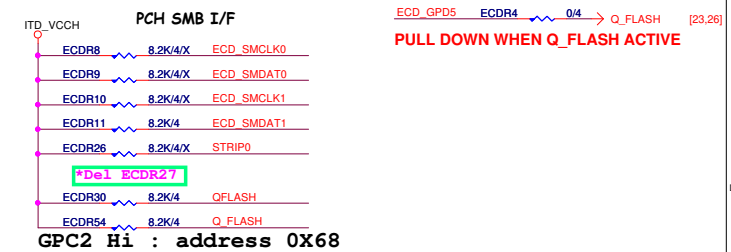


FRONT SIDE USB2.0

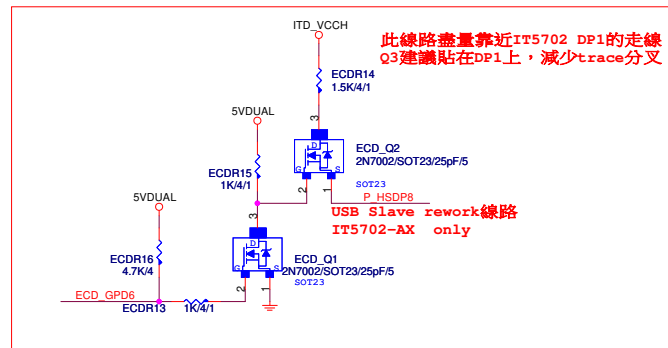
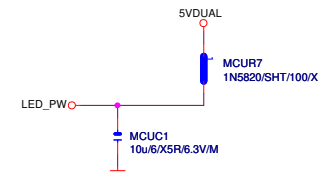
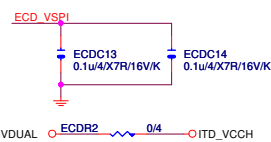


FROM CPU WITH O_FALSH



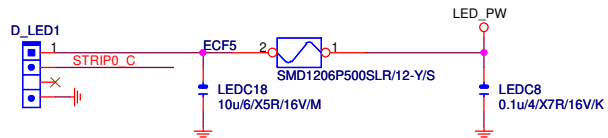


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[illegible]

第六區 LED (靠近左上板邊位置)

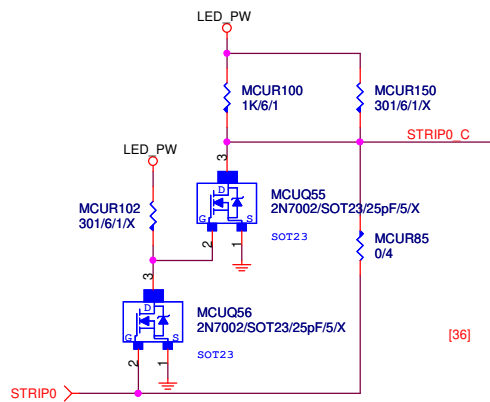
Digital LED Strip1



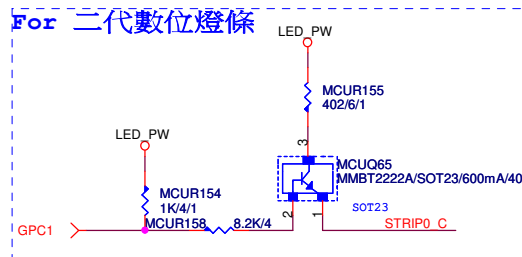
PH/1*4/BK/2.54/VA/D/[11NH2-000104-G1R]

Footprint PH1X4-CUT3-LED-L

燈條 Level shift



For 二代數位燈條



GIGABYTE™

Title

D_LED

Size

Custom

Document Number

A520M H

Rev

1.0

Date: Monday, May 18, 2020

Sheet 38 of 39

